Transient Voltage Suppressor Diode

BZA109TS

18 Diode Array

6.8V/100mA

DATASHEET

OEM – Philips

Source: Philips Databook 1999

9-fold ESD transient voltage suppressor BZA109TS

FEATURES

- ESD rating >8 kV, according to IEC1000-4-2
- SOT339-1 surface mount package
- Common anode configuration
- Non-clamping range –0.5 to +6.8 V
- Maximum non-repetitive peak reverse power dissipation: 25 W at t_p = 1 ms
- Maximum clamping voltage at peak pulse current: 10 V at I_{ZSM} = 2.5 A.

APPLICATIONS

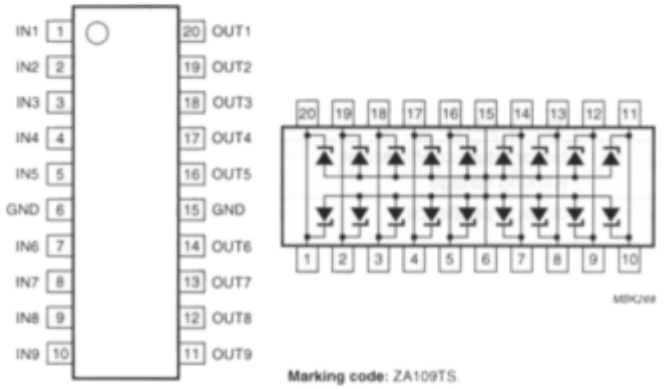
- For 9-bit wide undershoot/ overshoot clamping and fast ESD transient suppression in:
  - Computers and peripherals
  - Audio and video equipment
  - Business machines
  - Communication systems
  - Medical equipment.

DESCRIPTION

9-fold monolithic transient voltage suppressor in an SSOP20; SOT339-1 surface mount package. The device is ideal in situations where board space is a premium.

PINNING

PIN	DESCRIPTION
1 to 5	input (IN1 to IN5)
6 and 15	common anode (GND)
7 to 10	input (IN6 to IN9)
11 to 14	output (OUT9 to OUT6)
16 to 20	output (OUT5 to OUT1)



Marking code: ZA109TS.

Fig.1 Pin configuration for SSOP20 (SOT339-1) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per diode					
I_Z	working current	T_{amb} = 25 °C	–	20	mA
I_F	continuous forward current	T_{amb} = 25 °C	–	100	mA
I_{FT}	feed-through current	T_{amb} = 25 °C; note 1	–	100	mA
I_{FSM}	non-repetitive peak forward current	t_p = 1 ms; square pulse	–	4.5	A
I_{ZSM}	non-repetitive peak reverse current	t_p = 1 ms; square pulse; see Fig.2	–	2.5	A
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C; note 2; see Fig.3	–	0.95	W
P_{ZSM}	non-repetitive peak reverse power dissipation	t_p = 1 ms; square pulse; see Fig.4	–	25	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C

Notes

1. Current is flowing from input to corresponding output.
2. One or more diodes loaded.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	one or more diodes loaded	135	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per diode						
V_Z	working voltage	I_Z = 250 µA	6.4	6.8	7.2	V
V_F	forward voltage	I_F = 100 mA	–	–	1.1	V
V_{ZSM}	non-repetitive peak reverse voltage	I_{ZSM} = 2.5 A; t_p = 1 ms	–	–	10	V
I_H	input high current	V_{IN} = 5.25 V	–	–	0.5	µA
r_{dif}	differential resistance	I_Z = 250 µA	–	–	100	Ω
S_Z	temperature coefficient of working voltage	I_Z = 5 mA	–	3	–	mV/K
C_d	diode capacitance	see Fig.5				
		V_R = 0; f = 1 MHz	–	–	200	pF
		V_R = 5.25 V; f = 1 MHz	–	–	100	pF

GRAPHICAL DATA

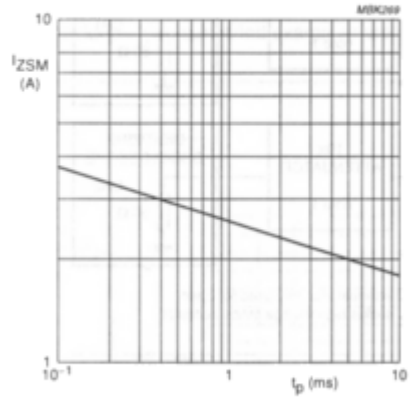
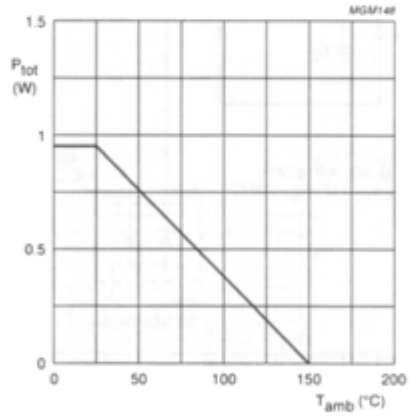
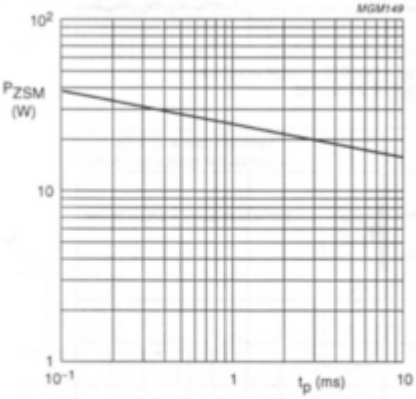


Fig.2 Maximum non-repetitive peak reverse current as a function of pulse time.



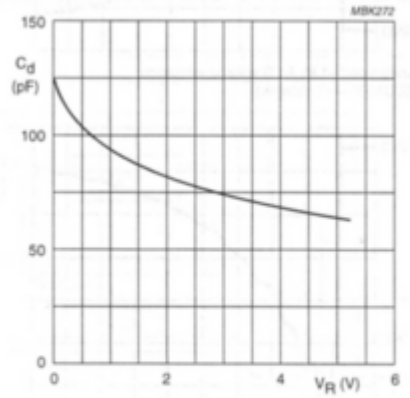
One or more diodes loaded.

Fig.3 Power derating curve.



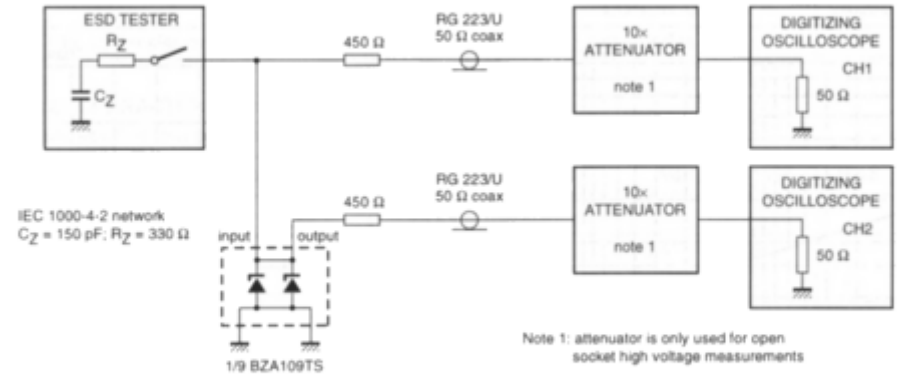
$P_{ZSM} = V_{ZSM} \times I_{ZSM}$.
V_{ZSM} is the non-repetitive peak reverse voltage at I_{ZSM}.

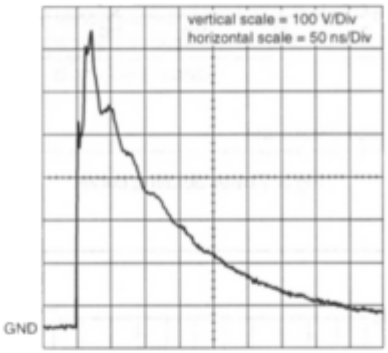
Fig.4 Maximum non-repetitive peak reverse power dissipation as a function of pulse duration (square pulse).



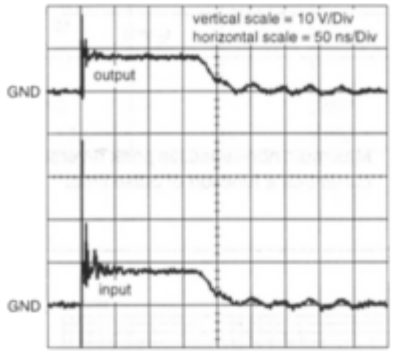
T_j = 25 °C; f = 1 MHz.

Fig.5 Diode capacitance as a function of reverse voltage; typical values.

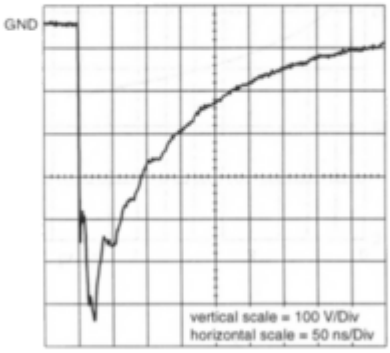




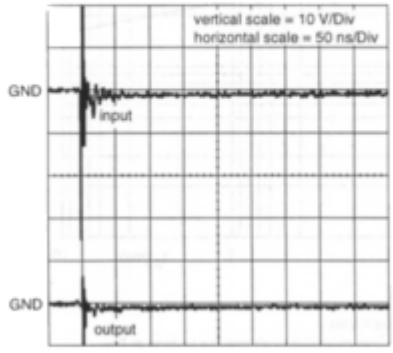
unclamped +1 kV ESD voltage waveform (IEC1000–4–2 network)



clamped +1 kV ESD voltage waveform (IEC1000–4–2 network)



unclamped −1 kV ESD voltage waveform (IEC1000–4–2 network)



clamped −1 kV ESD voltage waveform (IEC1000–4–2 network)

MBK382

Fig.6 ESD clamping test set-up and waveforms.

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APPLICATION INFORMATION

Typical common anode application

A 9-fold transient suppressor in an SSOP20; SOT339-1 package makes it possible to protect nine separate lines using only one package. Two simplified examples are shown in Figs 7 and 8.

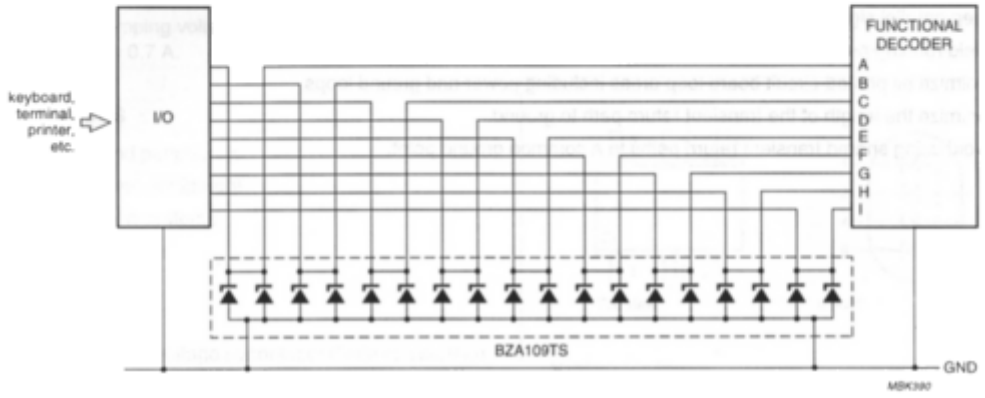

Fig.7 Computer interface protection.

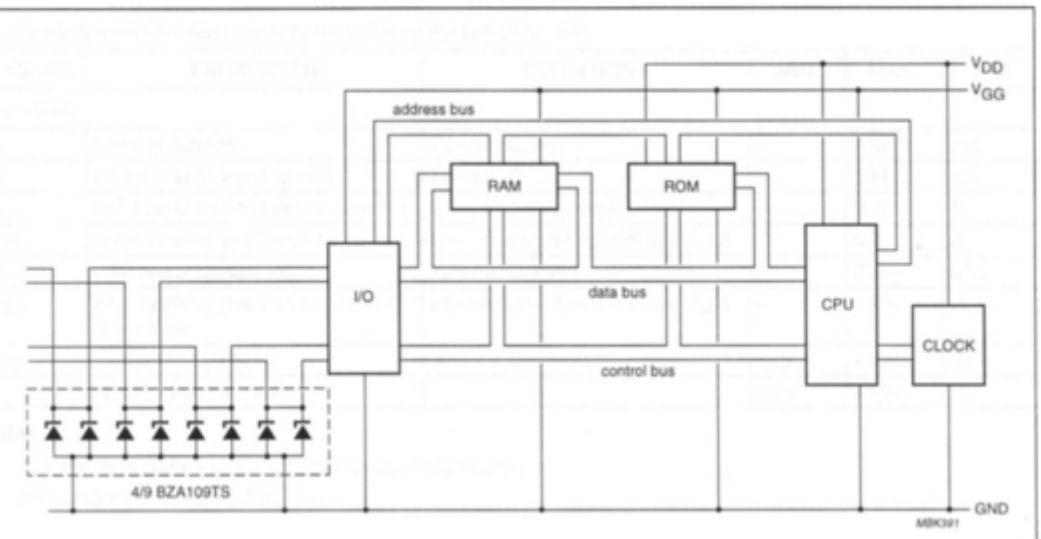

Fig.8 Microprocessor protection.

Device placement and printed-circuit board layout

Circuit board layout is of extreme importance in the suppression of transients. The clamping voltage of the BZA109TS is determined by the peak transient current and the rate of rise of that current (di/dt). Since parasitic inductances can further add to the clamping voltage (V = L di/dt) the series conductor lengths on the printed-circuit board should be kept to a minimum. This includes the lead length of the suppression element.

In addition to minimizing conductor length the following printed-circuit board layout guidelines are recommended:

1. Place the suppression element close to the input terminals or connectors.
2. Keep parallel signal paths to a minimum.
3. Avoid running protection conductors in parallel with unprotected conductors.
4. Minimize all printed-circuit board loop areas including power and ground loops.
5. Minimize the length of the transient return path to ground.
6. Avoid using shared transient return paths to a common ground point.