

# AD - Converter

## ICL7136

Single Chip AD – Converter

# DATASHEET

OEM – Intersil

*Source: Intersil Databook 1987*

# ICL7136

## 3 1/2-Digit LCD Low Power A/D Converter



ICL7136

### GENERAL DESCRIPTION

The Intersil ICL7136 is a high performance, very low power 3 1/2-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7136 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is under 100µA, ideally suited for 9V battery operation.

The 7136 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10µV, zero drift of less than 1µV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

The ICL7136 is an improved version of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

### FEATURES

- First-Reading Recovery From Overrange Gives Immediate "OHMS" Measurement
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct LCD Display Drive — No External Components Required
- Pin Compatible With The ICL7106, ICL7126
- Low Noise — 15µVp-p Without Hysteresis or Overrange Hangover
- On-Chip Clock and Reference
- Low Power Dissipation, Guaranteed Less Than 1mW — Gives 8,000 Hours Typical 9V Battery Life
- No Additional Active Circuits Required
- Evaluation Kit Available (ICL7136EV/Kit)

### ORDERING INFORMATION

| Part Number   | Temperature Range | Package              |
|---------------|-------------------|----------------------|
| ICL7136CM44   | 0°C to +70°C      | 44-Pin Surface Mount |
| ICL7136CPL    | 0°C to +70°C      | 40-Pin Plastic DIP   |
| ICL7136RCPL   | 0°C to +70°C      | 40-Pin Plastic DIP   |
| ICL7136EV/KIT |                   | EVALUATION KIT       |

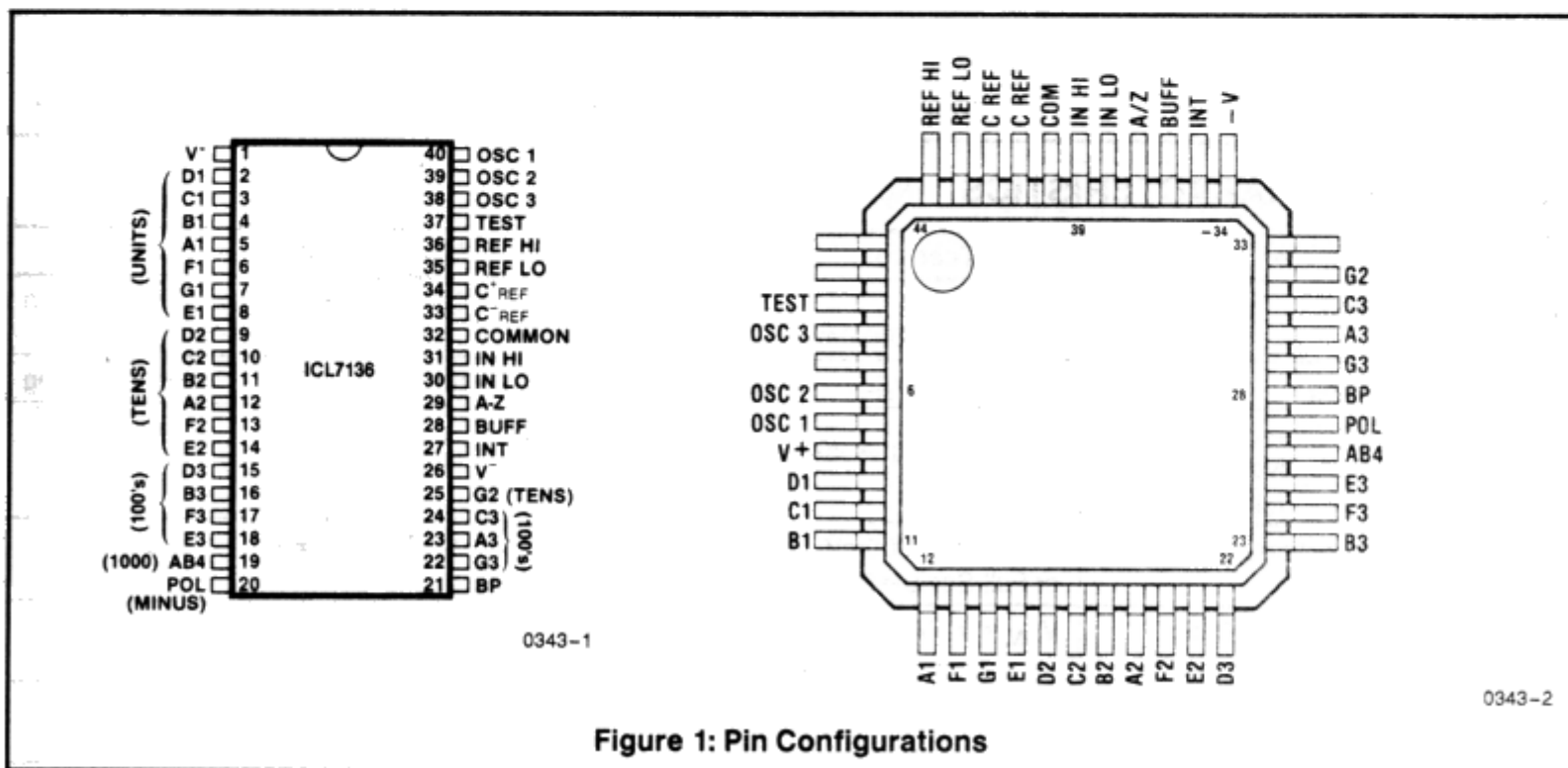


Figure 1: Pin Configurations

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**ICL7136**  
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**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (V<sup>+</sup> to V<sup>-</sup>) ..... 15V  
 Analog Input Voltage (either input)(Note 1) ..... V<sup>+</sup> to V<sup>-</sup>  
 Reference Input Voltage (either input) ..... V<sup>+</sup> to V<sup>-</sup>  
 Clock Input ..... TEST to V<sup>+</sup>

Power Dissipation (Note 2)  
 Ceramic Package ..... 1000mW  
 Plastic Package ..... 800mW  
 Operating Temperature ..... 0°C to +70°C  
 Storage Temperature ..... -65°C to +150°C  
 Lead Temperature (Soldering, 10sec) ..... 300°C

**Note 1:** Input voltages may exceed the supply voltages, provided the input current is limited to ±100µA.

**Note 2:** Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

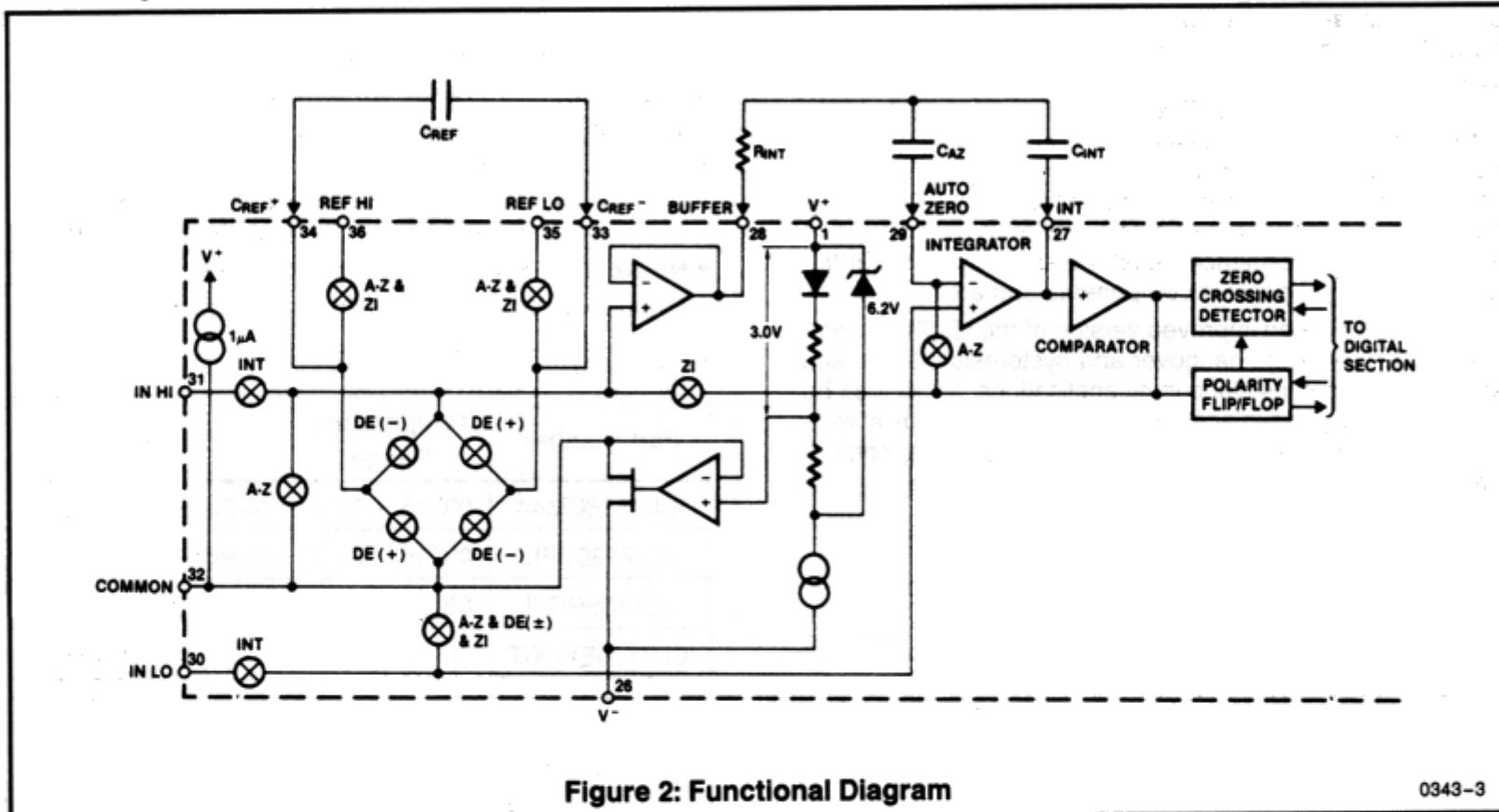


Figure 2: Functional Diagram

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**ELECTRICAL CHARACTERISTICS** (Notes 3, 7)

| Parameter   | Test Conditions   | Min    | Typ      | Max    | Unit            |
|---|---|--------|----------|--------|-----------------|
| Zero Input Reading  | V <sub>IN</sub> = 0.0V<br>Full-Scale = 200.0mV                      | -000.0 | ±000.0   | +000.0 | Digital Reading |
| Ratiometric Reading   | V <sub>IN</sub> = V <sub>REF</sub> , V <sub>REF</sub> = 100mV       | 999    | 999/1000 | 1000   | Digital Reading |
| Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale) | -V <sub>IN</sub> = +V <sub>IN</sub> ≈ 200.0mV                       | -1     | ±0.2     | +1     | Counts          |
| Linearity (Max. deviation from best straight line fit)  | Full-scale = 200mV<br>or Full-Scale = 2.000V                        | -1     | ±0.02    | +1     | Counts          |
| Common-Mode Rejection Ratio (Note 4)  | V <sub>CM</sub> = ±1V, V <sub>IN</sub> = 0V<br>Full-Scale = 200.0mV |        | 50       |        | µV/V            |
| Noise (Pk-Pk value not exceeded 95% of time)  | V <sub>IN</sub> = 0V, Full Scale = 200.0mV                          |        | 15       |        | µV              |
| Leakage Current @ Input   | V <sub>IN</sub> = 0V  |        | 1        | 10     | pA              |

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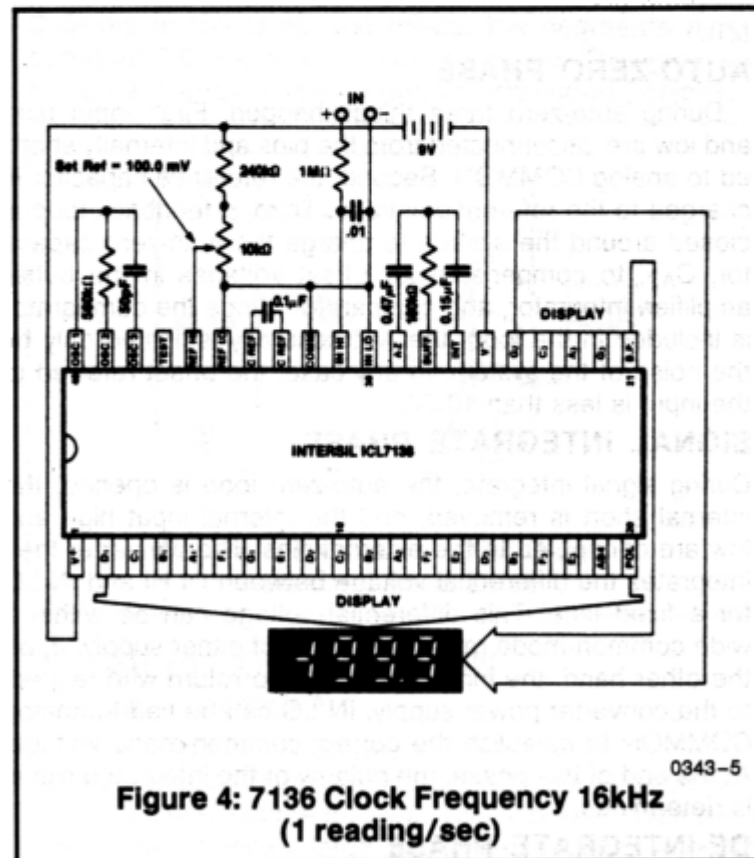
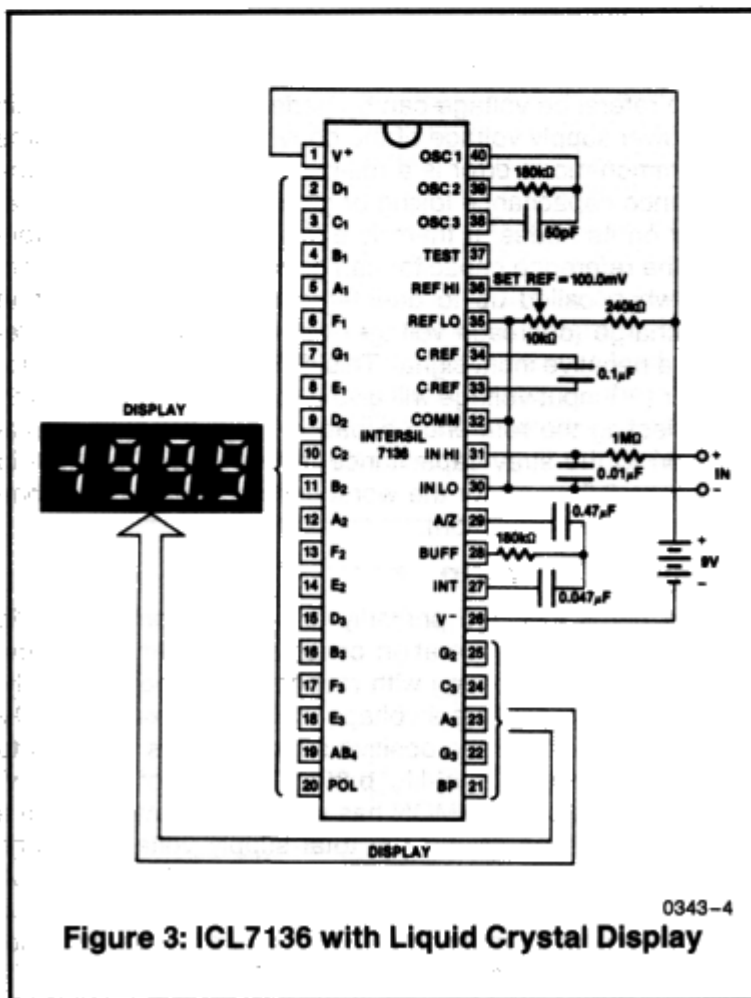
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## ELECTRICAL CHARACTERISTICS (Notes 3, 7) (Continued)

| Parameter   | Test Conditions   | Min | Typ | Max | Unit              |
|---|---|-----|-----|-----|-------------------|
| Zero Reading Drift  | $V_{IN} = 0V, 0^{\circ}C < T_A < +70^{\circ}C$  |     | 0.2 | 1   | $\mu V/^{\circ}C$ |
| Scale Factor Temperature Coefficient                            | $V_{IN} = 199.0mV, 0^{\circ}C < T_A < +70^{\circ}C$<br>(Ext. Ref. Oppm/ $^{\circ}C$ ) |     | 1   | 5   | ppm/ $^{\circ}C$  |
| Supply Current (Does not include COMMON current)                | $V_{IN} = 0V$ (Note 6)  |     | 70  | 100 | $\mu A$           |
| Analog COMMON Voltage (With respect to positive supply)         | 250k $\Omega$ between Common and Positive Supply                                      | 2.4 | 2.8 | 3.2 | V                 |
| Temp. Coeff. of Analog COMMON (With respect to positive supply) | 250k $\Omega$ between Common and Positive Supply                                      |     | 150 |     | ppm/ $^{\circ}C$  |
| Pk-Pk Segment Drive Voltage (Note 5)                            | $V^+$ to $V^- = 9V$   | 4   | 5   | 6   | V                 |
| Pk-Pk Backplane Drive Voltage (Note 5)                          | $V^+$ to $V^- = 9V$   | 4   | 5   | 6   | V                 |
| Power Dissipation Capacitance                                   | vs Clock Frequency  |     | 40  |     | pF                |

- NOTES:**
- Unless otherwise noted, specifications apply at  $T_A = 25^{\circ}C$ ,  $f_{clock} = 16kHz$  and are tested in the circuit of Figure 4.
  - Refer to "Differential Input" discussion.
  - Backplane drive is in phase with segment drive for "off" segment, 180 $^{\circ}$  out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
  - 48kHz oscillator, Figure 5, increases current by 20 $\mu A$  (typ).
  - Extra capacitance of Cerdip package changes oscillator resistor value to 470k $\Omega$  or 150k $\Omega$  (1 reading/sec or 3 readings/sec).

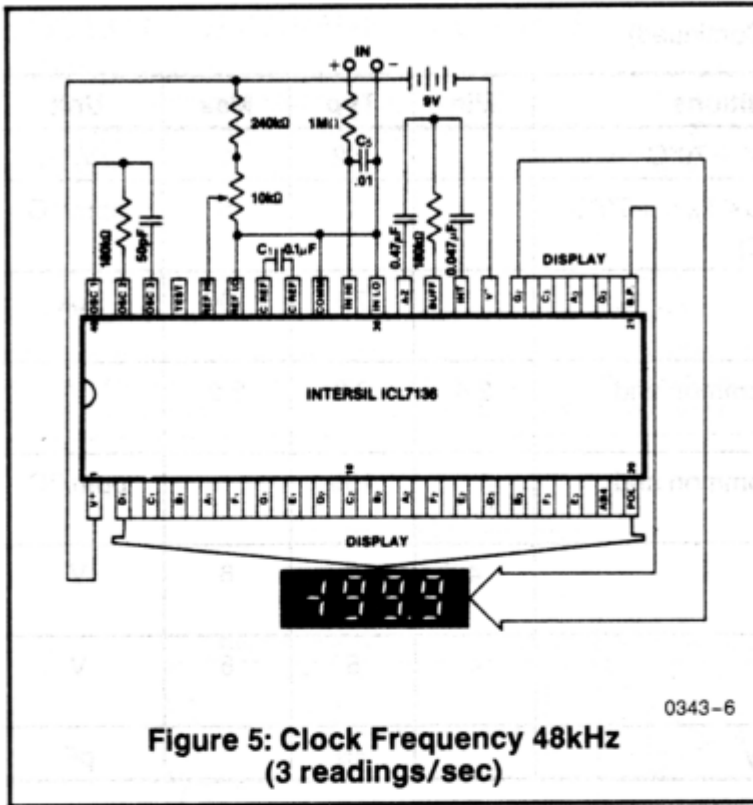
## TEST CIRCUITS



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**Figure 5: Clock Frequency 48kHz  
(3 readings/sec)**

**DETAILED DESCRIPTION  
(Analog Section)**

Figure 2 shows the Functional Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

**AUTO-ZERO PHASE**

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor,  $C_{AZ}$ , to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than  $10\mu V$ .

**SIGNAL INTEGRATE PHASE**

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

**DE-INTEGRATE PHASE**

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the

capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is  $1000 (V_{IN}/V_{REF})$ .

**ZERO INTEGRATOR PHASE**

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

**Differential Input**

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

**Differential Reference**

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection).

**Analog Common**

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ( $> 7V$ ), the COMMON voltage will have a low voltage coefficient ( $0.001\%/%$ ), low output impedance ( $\approx 35\Omega$ ), and a temperature coefficient typically less than  $150ppm/^{\circ}C$ .

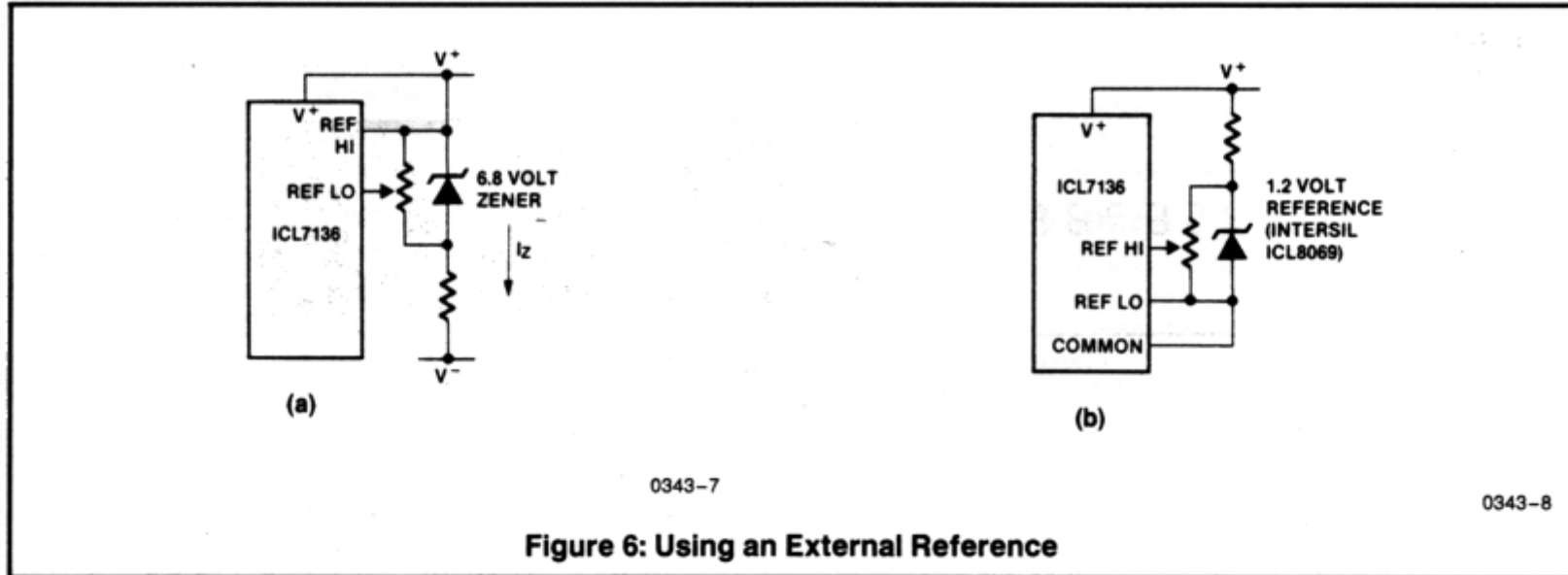
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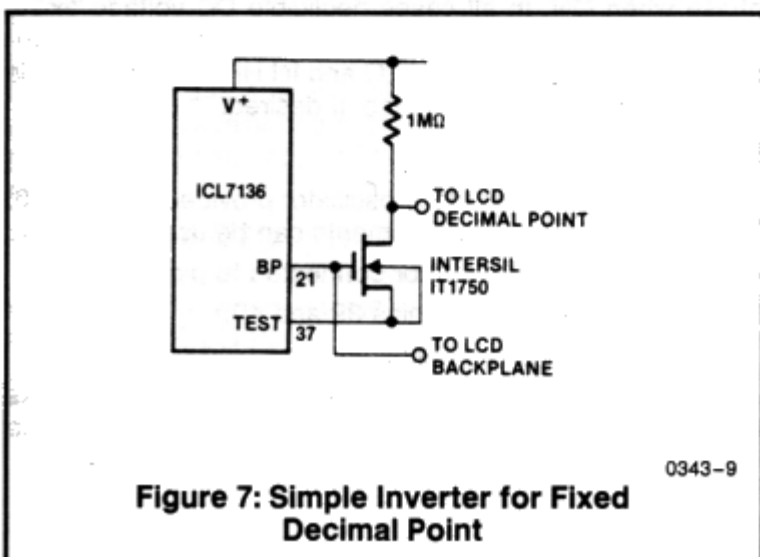
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The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 3mA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1µA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

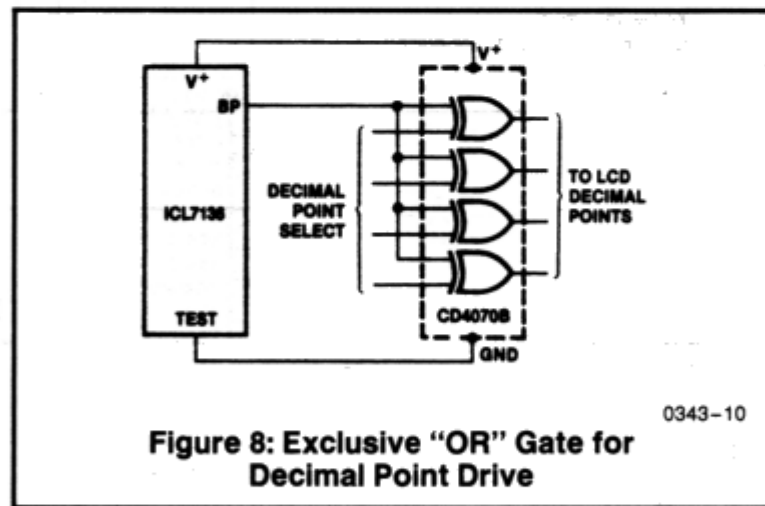


## TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus, it can be used as the negative supply for external segment drivers such as for decimal points or any other presentation the user may want to include on the LCD display. Figures 7 and 8 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V+) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10mA under these conditions.

**Caution: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.**



## DETAILED DESCRIPTION (Digital Section)

Figure 9 shows the digital section for the 7136. An internal digital ground is generated from a 6V Zener diode and a large P channel source follower. This supply is made stiff to absorb the relatively large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and

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**ICL7136**  
**DISPLAY FONT**

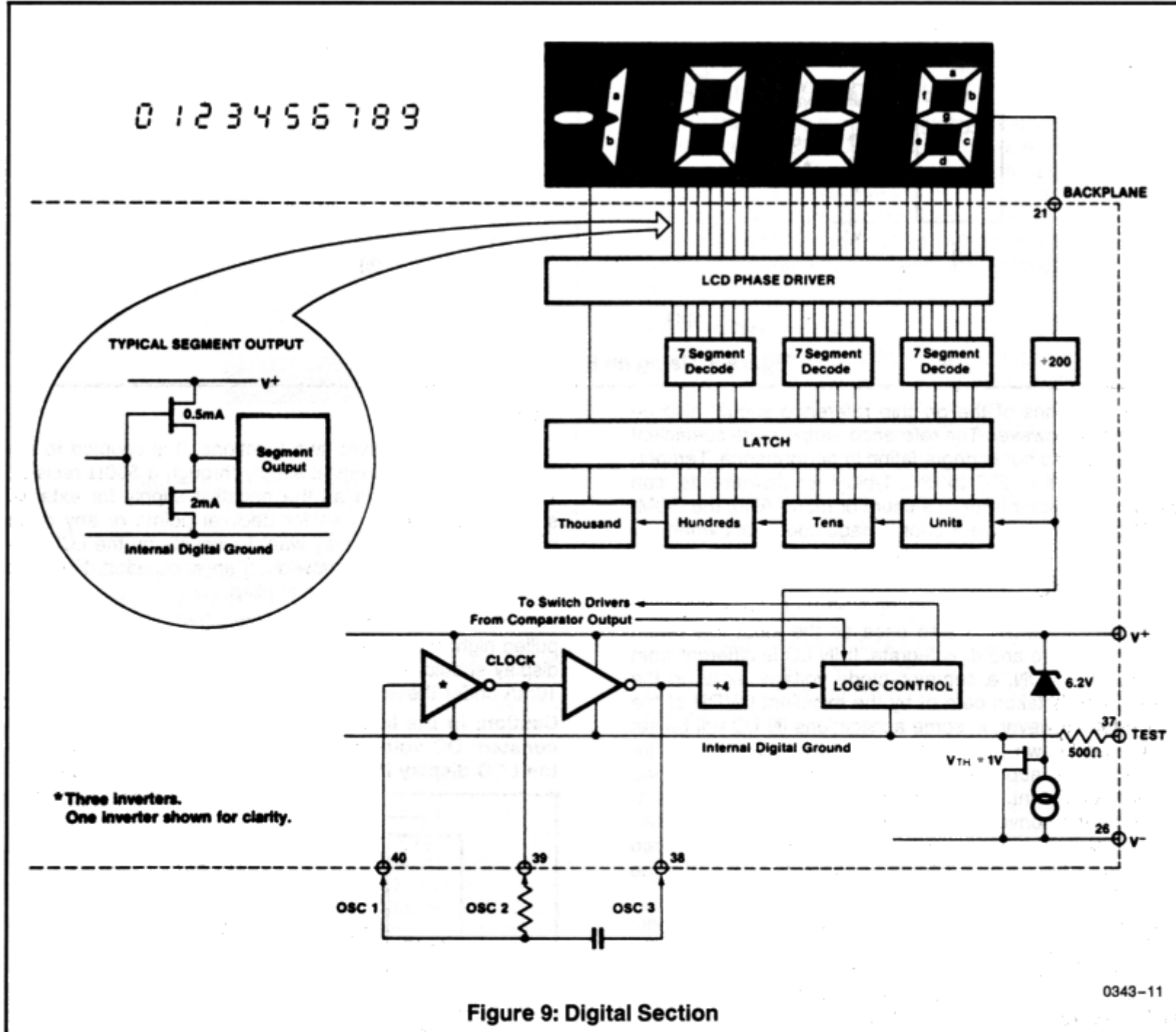


Figure 9: Digital Section

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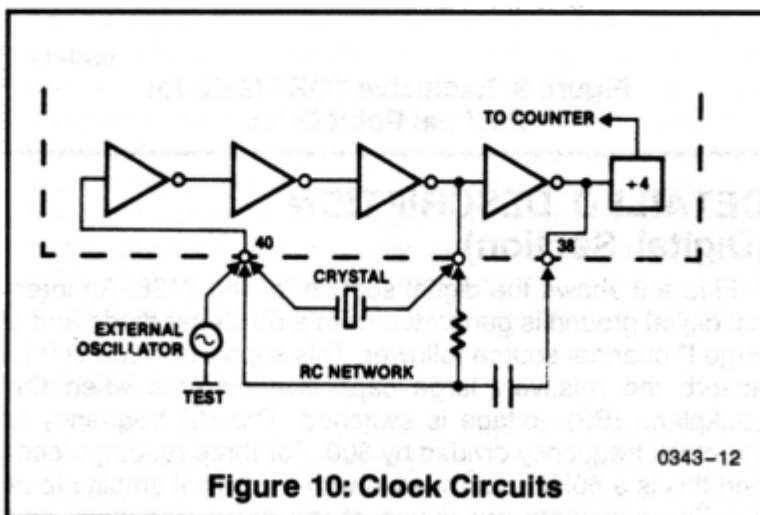


Figure 10: Clock Circuits

0343-12

amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

**System Timing**

Figure 10 shows the clock oscillator provided in the 7136. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the

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four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts\*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66 2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz). See also A052.

## COMPONENT VALUE SELECTION

(See also A052)

### Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

### Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C<sub>INT</sub> are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

### Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7126 or ICL7106 (see A032).

### Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

\*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

## Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation  $f \sim 0.45/RC$ . For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

## Reference Voltage

The analog input required to generate full-scale output (2000 counts) is  $V_{IN} = 2V_{REF}$ . Thus, for the 200.0mV and 2.000V scale,  $V_{REF}$  should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select  $V_{REF} = 0.341V$ . A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for  $V_{IN} \neq 0$ . Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

## TYPICAL APPLICATIONS

The 7136 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

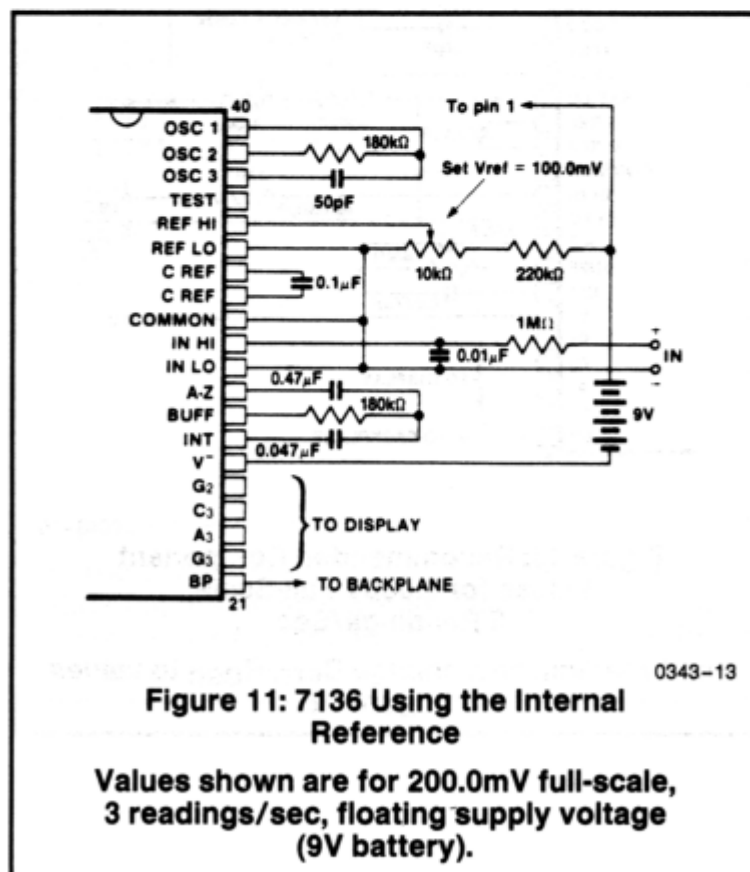


Figure 11: 7136 Using the Internal Reference

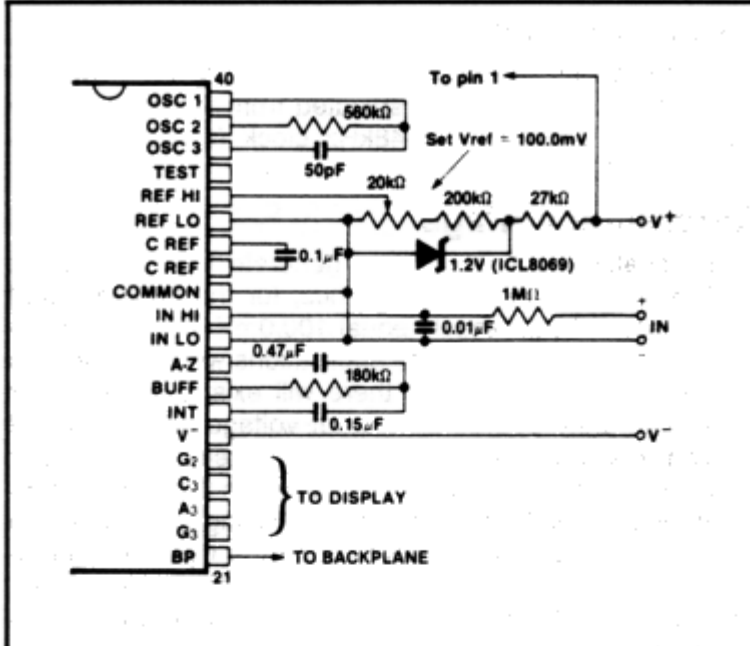
Values shown are for 200.0mV full-scale, 3 readings/sec, floating supply voltage (9V battery).

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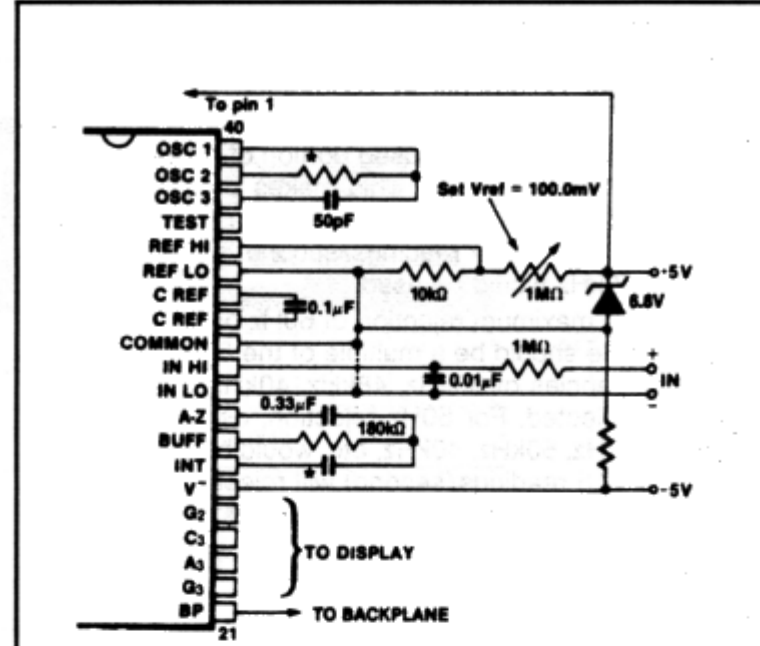
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Figure 12: 7136 with an External Band-Gap Reference (1.2V Type)

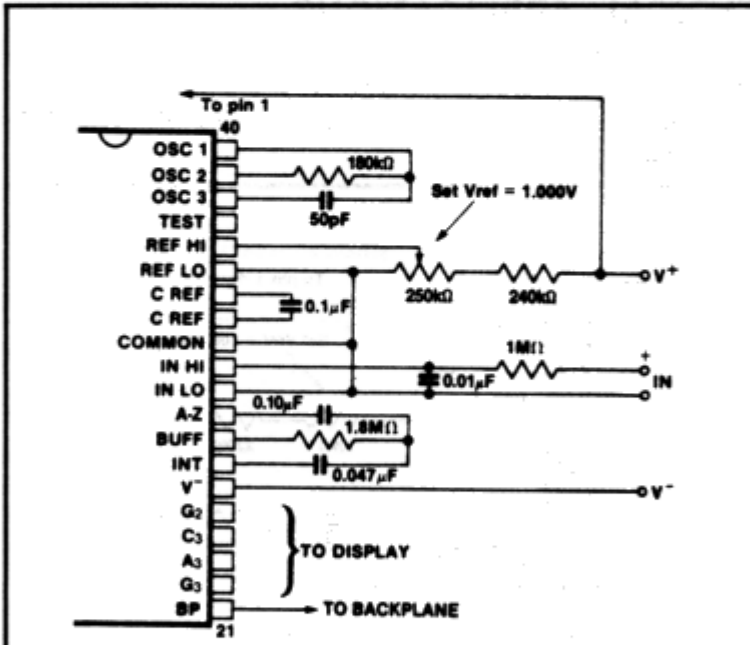
IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.



0343-16

Figure 14: 7136 with Zener Diode Reference

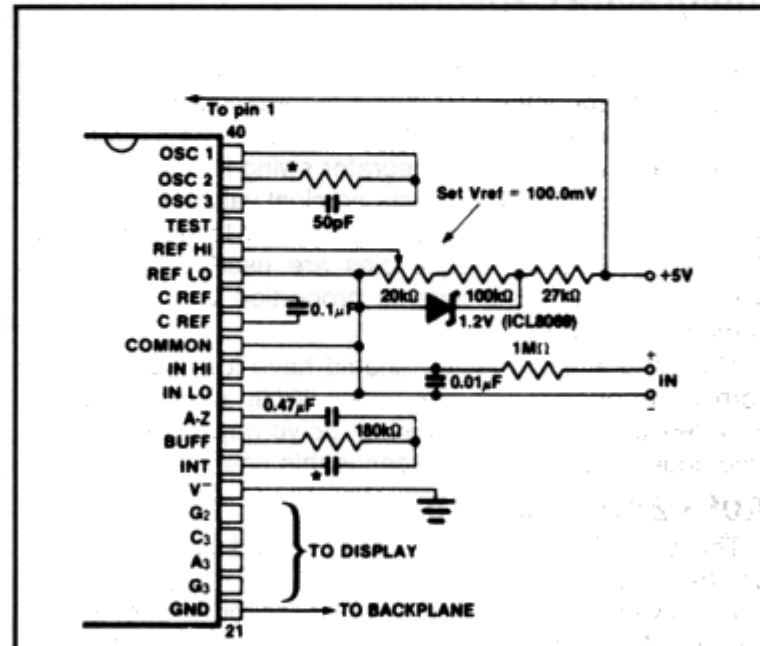
Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 13, IN LO may be tied to COMMON.



0343-15

Figure 13: Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec

For 1 reading/sec, change C<sub>INT</sub>, R<sub>OSC</sub> to values of Figure 12.



0343-17

Figure 15: 7136 Operated from Single +5V Supply

An external reference must be used in this application, since the voltage between V<sup>+</sup> and V<sup>-</sup> is insufficient for correct operation of the internal reference.

\*Values depend on clock frequency. See Figures 11, 12, 13.

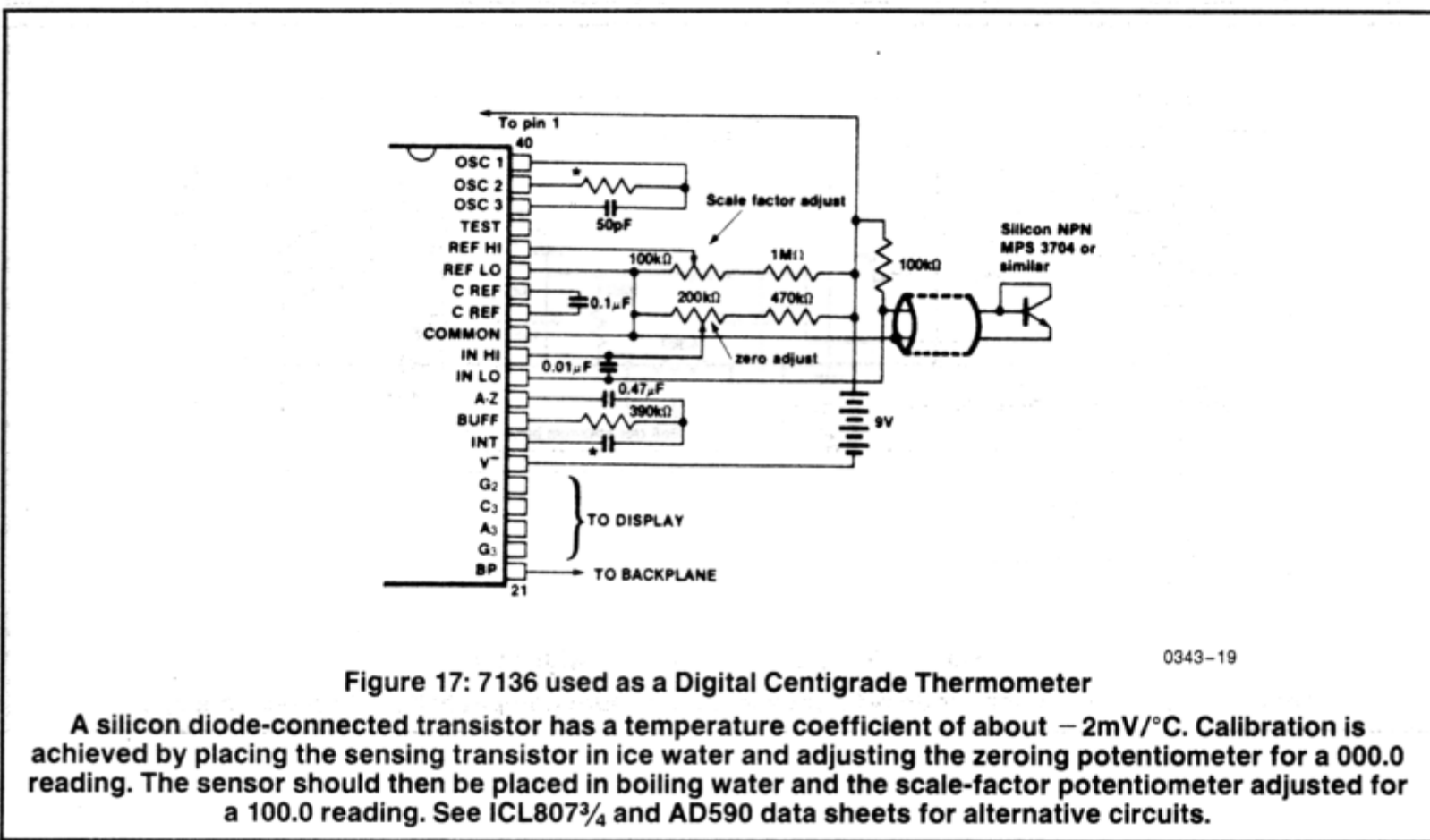
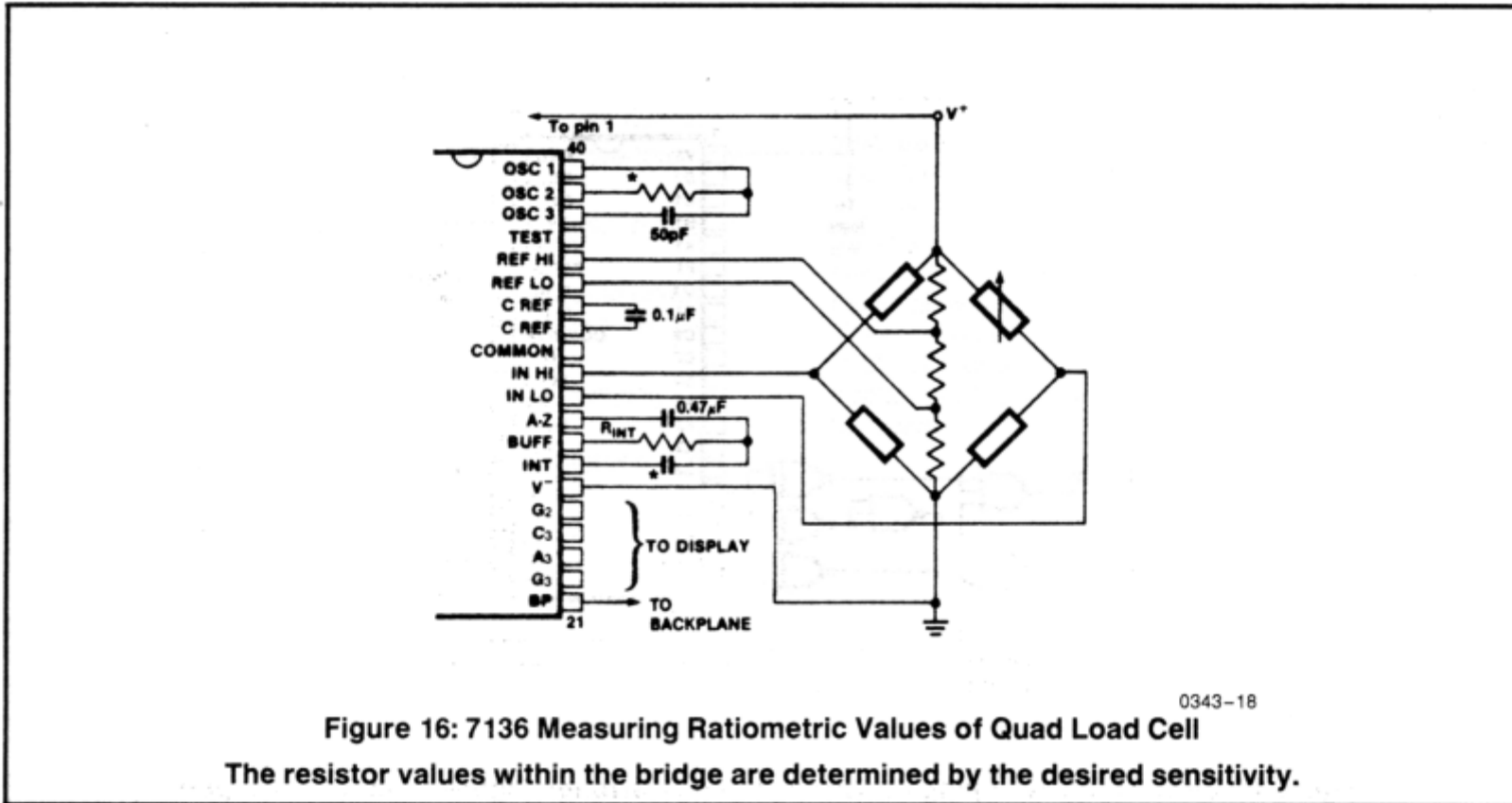
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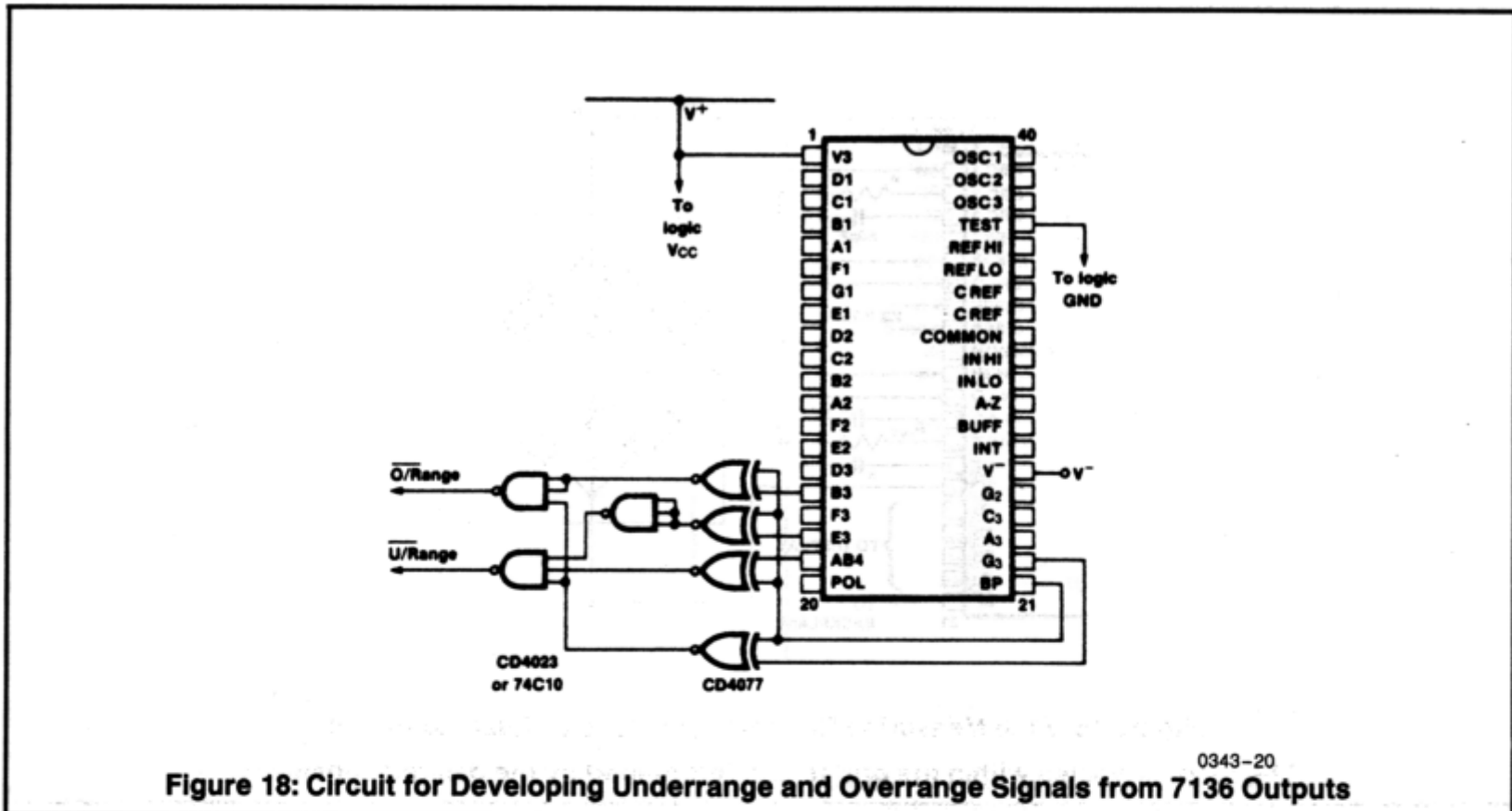
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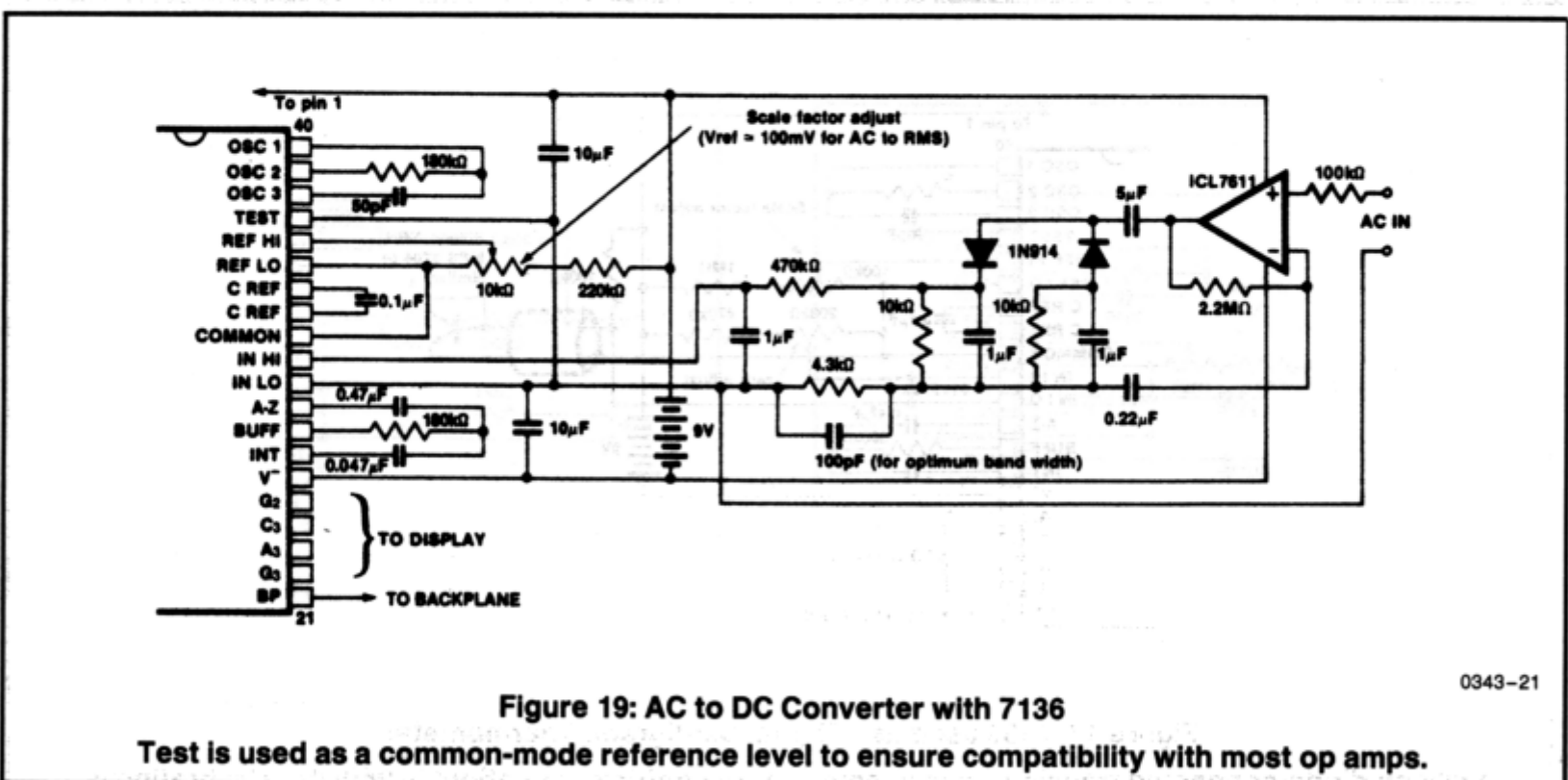
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**Figure 18: Circuit for Developing Underrange and Overrange Signals from 7136 Outputs**



0343-21  
**Figure 19: AC to DC Converter with 7136**  
Test is used as a common-mode reference level to ensure compatibility with most op amps.

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NOTE: All typical values have been characterized but are not tested.

## ICL7136

**INTERSIL****ICL7136**

### APPLICATION NOTES

- A016** "Selecting A/D Converters," by David Fullagar.
- A017** "The Integrating A/D Converter," by Lee Evans.
- A018** "Do's and Don't's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- A023** "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
- A032** "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
- A046** "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
- A047** "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.
- A052** "Tips for Using Single-Chip 3 $\frac{1}{2}$ -Digit A/D Converters," by Dan Watson.

### 7136 EVALUATION KIT

After purchasing a sample of the 7136, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3 $\frac{1}{2}$ -digit panel meter. With the ICL7136EV/Kit and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

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*NOTE: All typical values have been characterized but are not tested.*