

AD - Converter

ICL7135

4 ½ digit BCD out AD – Converter

DATASHEET

OEM – Intersil

Source: Intersil Databook 1987

ICL7135 4 1/2-Digit BCD Output A/D Converter



GENERAL DESCRIPTION

The Intersil ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ± 1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS I.C., with the exception of display drivers, reference, and a clock.

The Intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than $10\mu\text{V}$, zero drift of less than $1\mu\text{V}/^\circ\text{C}$, input bias current of 10 pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include STROBE, OVERRANGE, UNDER-RANGE, RUN/HOLD and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

FEATURES

- Accuracy Guaranteed to ± 1 Count Over Entire $\pm 20,000$ Counts (2.0000 Volts Full Scale)
- Guaranteed Zero Reading for 0 Volts Input
- 1 pA Typical Input Current
- True Differential Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage Required
- Over-Range and Under-Range Signals Available for Auto-Range Capability
- All Outputs TTL Compatible
- Blinking Outputs Gives Visual Indication of Over-range
- Six Auxiliary Inputs/Outputs Are Available for Interfacing to UARTs, Microprocessors or Other Circuitry
- Multiplexed BCD Outputs

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7135CJI	0°C to +70°C	28-Pin Cerdip
ICL7135CPI	0°C to +70°C	28-Pin Plastic Dip
ICL7135EV/KIT	Evaluation Kit (PC Board, active, passive components)	

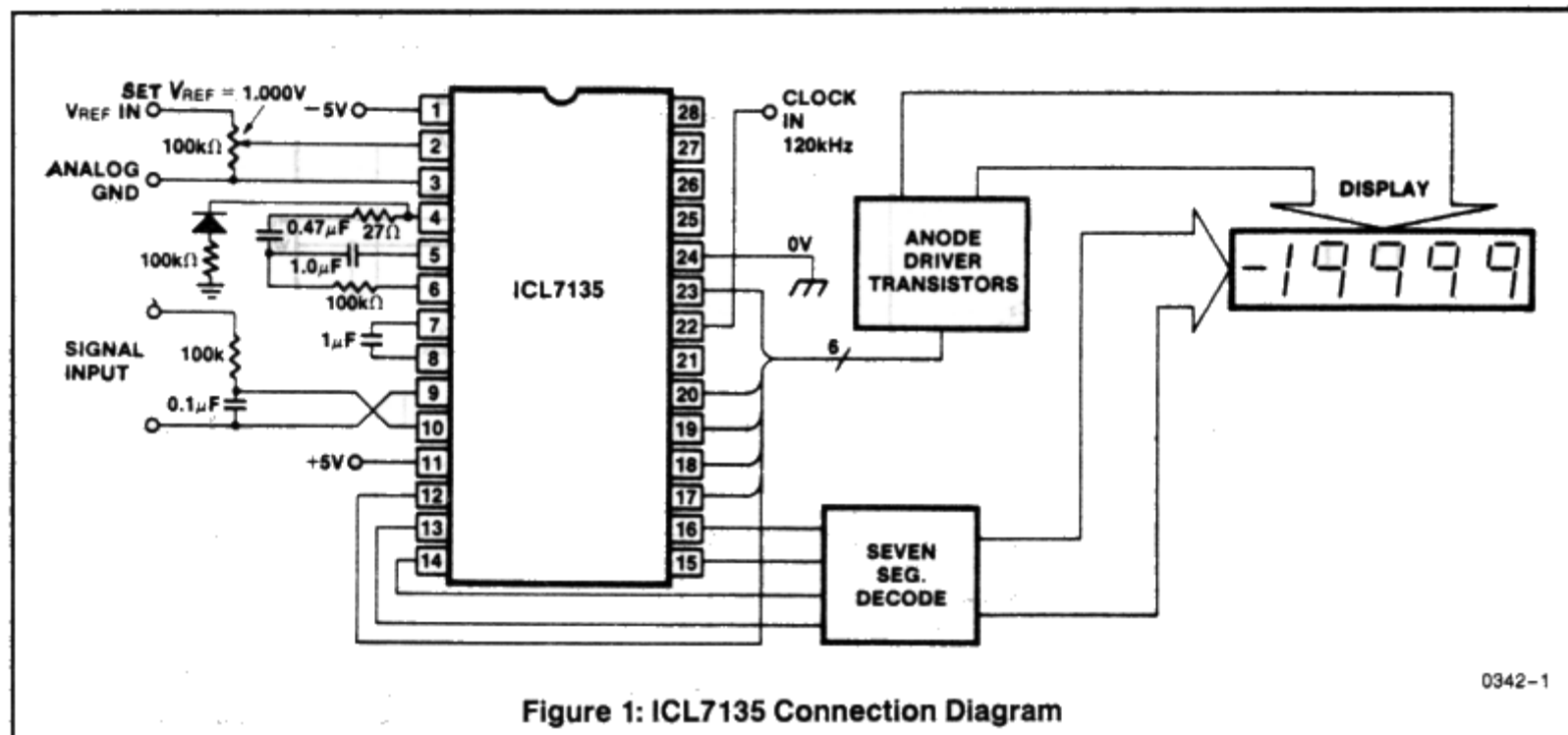


Figure 1: ICL7135 Connection Diagram

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+	+6V	Power Dissipation (Note 2)	
V^-	-9V	Ceramic Package	1000mW
Analog Input Voltage (either input) (Note 1)	V^+ to V^-	Plastic Package	800mW
Reference Input Voltage (either input)	V^+ to V^-	Operating Temperature	0°C to +70°C
Clock Input	Gnd to V^+	Storage Temperature	-65°C to +150°C
		Lead Temperature (Soldering, 10sec)	300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100 μ A.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

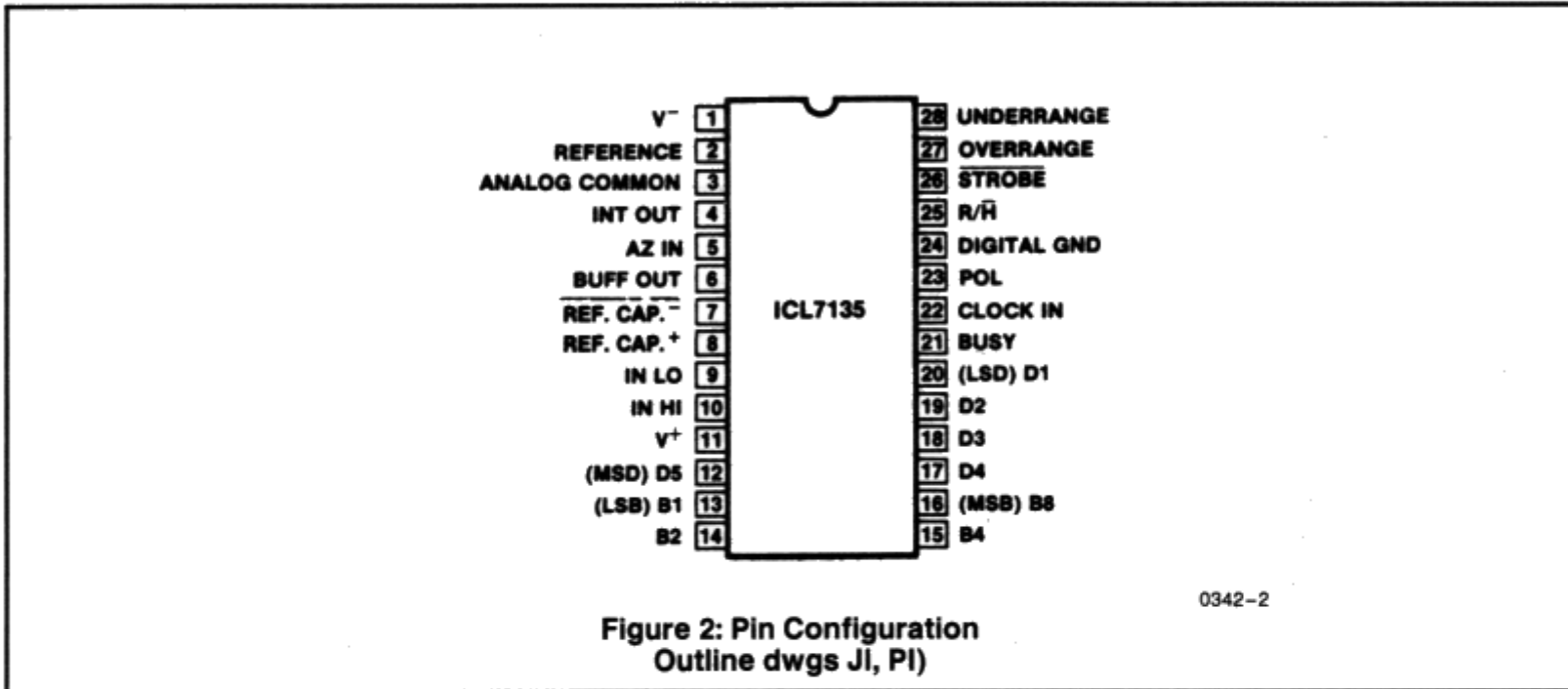


Figure 2: Pin Configuration Outline dwgs JI, PI)

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ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25^\circ C$, Clock Frequency Set for 3 Reading/Sec)

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
ANALOG (Note 1) (Note 2)						
	Zero Input Reading	$V_{IN} = 0.0V$ Full Scale = 2.000V	-0.0000	± 0.0000	+0.0000	Digital Reading
	Ratiometric Reading (2)	$V_{IN} \equiv V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
	Linearity over \pm Full Scale (error of reading from best straight line)	$-2V \leq V_{IN} \leq +2V$		0.5	1	Digital Count Error
	Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-2V \leq V_{IN} \leq +2V$.01		LSB
	Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error

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ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25^\circ C$, Clock Frequency Set for 3 Reading/Sec) (Continued)

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit	
e_n	Noise (P-P value not exceeded 95% of time)	$V_{IN} = 0V$ Full scale = 2.000V		15		μV	
I_{ILK}	Leakage Current at Input	$V_{IN} = 0V$		1	10	pA	
	Zero Reading Drift	$V_{IN} = 0V$ $0^\circ \leq T_A \leq 70^\circ C$		0.5	2	$\mu V/^\circ C$	
TC	Scale Factor Temperature Coefficient (3)	$V_{IN} = +2V$ $0 \leq T_A \leq 70^\circ C$ (ext. ref. 0 ppm/ $^\circ C$)		2	5	ppm/ $^\circ C$	
DIGITAL							
INPUTS							
V_{INH} V_{INL} I_{INL} I_{INH}	Clock in, Run/Hold, See Figure 4	$V_{IN} = 0$ $V_{IN} = +5V$	2.8	2.2		V	
				1.6	0.8		
				0.02	0.1		mA
				0.1	10		μA
OUTPUTS							
V_{OL} V_{OH} V_{OH}	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5 BUSY, STROBE, OVER-RANGE, UNDER-RANGE POLARITY	$I_{OL} = 1.6mA$ $I_{OH} = -1mA$ $I_{OH} = -10\mu A$		0.25	0.40	V	
			2.4	4.2		V	
			4.9	4.99		V	
SUPPLY							
V^+	+5V Supply Range		+4	+5	+6	V	
V^-	-5V Supply Range		-3	-5	-8	V	
I^+	+5V Supply Current	$f_c = 0$		1.1	3.0	mA	
I^-	-5V Supply Current	$f_c = 0$		0.8	3.0		
C_{PD}	Power Dissipation Capacitance	vs. Clock Freq		40		pF	
CLOCK							
	Clock Freq. (Note 4)		DC	2000	1200	kHz	

NOTES: 1. Tested in 4-1/2 digit (20,000 count) circuit shown in Figure 3, clock frequency 120kHz.

2. Tested with a low dielectric absorption integrating capacitor and $R_{INT} = 0$. See Component Selection Section.

3. The temperature range can be extended to $+70^\circ C$ and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

4. This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" section for limitations on the clock frequency range in a system.

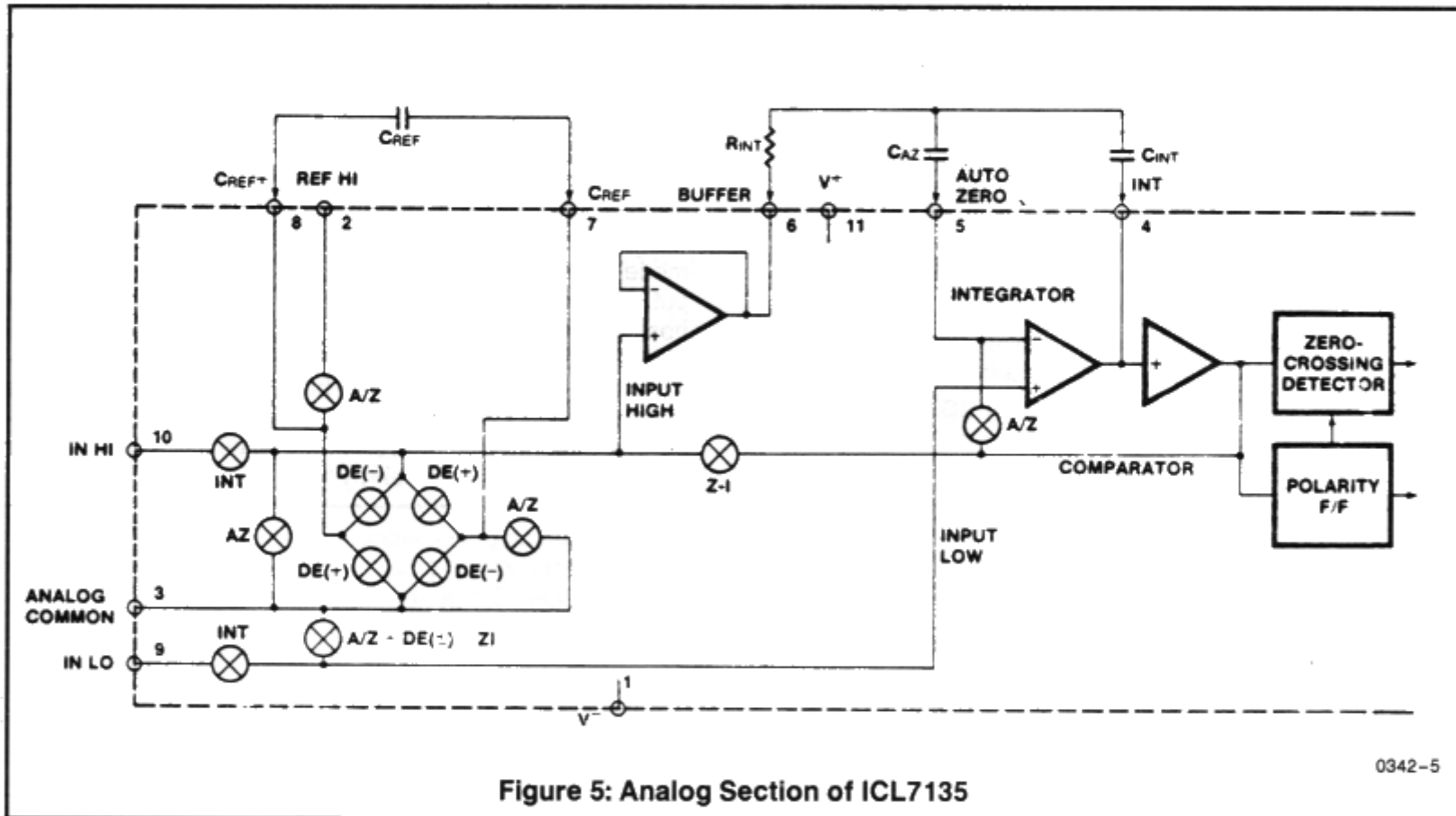
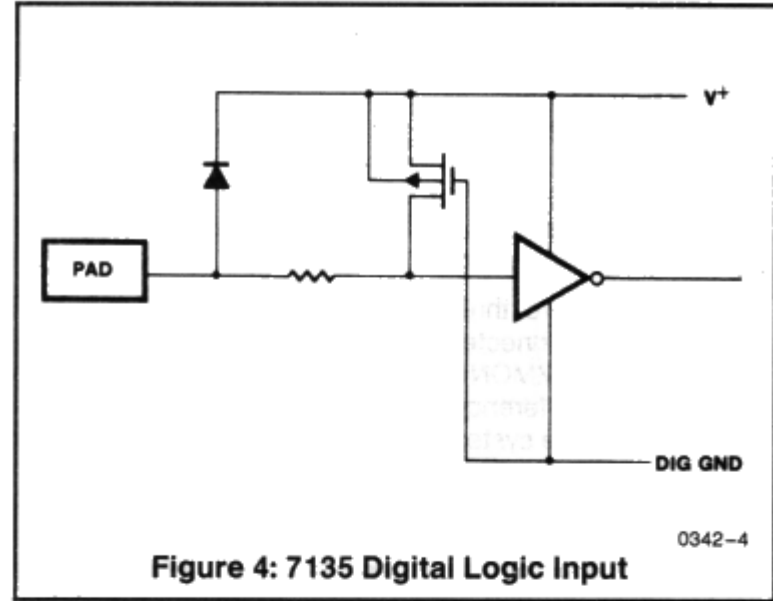
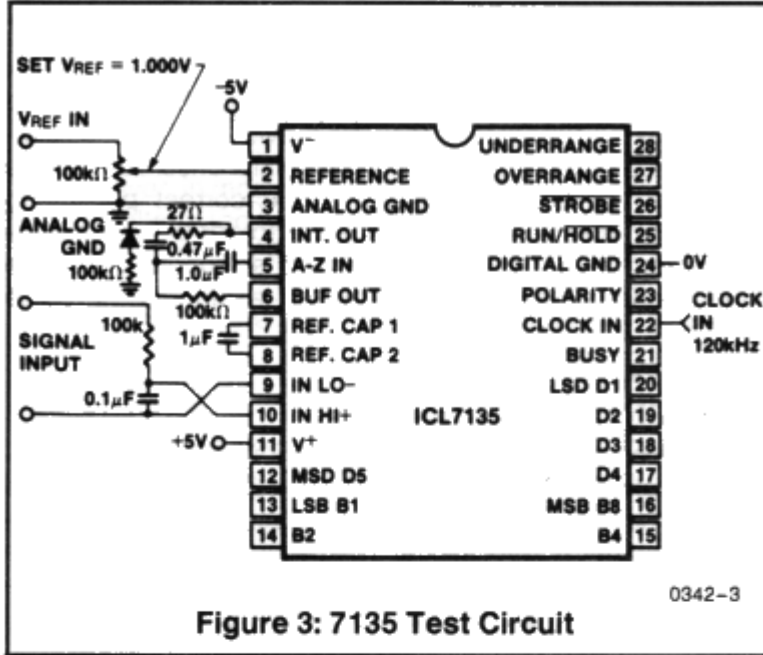
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DETAILED DESCRIPTION

Analog Section

Figure 5 shows the Block Diagram of the Analog Section for the ICL7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal-integrate (INT), (3) deintegrate (DE) and (4) zero-integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F/F.

DE-INTEGRATE PHASE

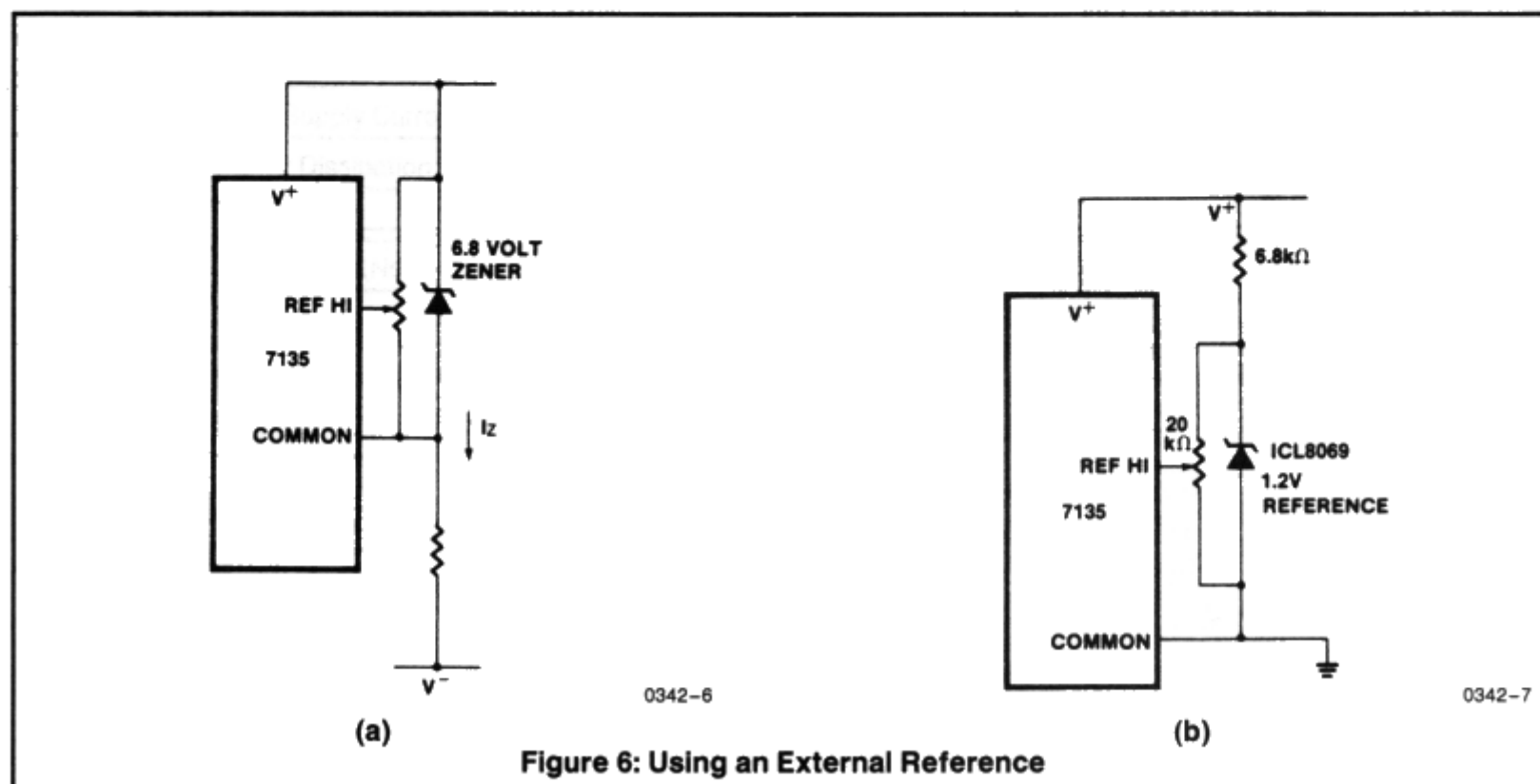
The Third phase is de-integrate, or reference integrate. Input LOW is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $10,000 \left(\frac{V_{IN}}{V_{REF}} \right)$.

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.



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Analog Common

Analog COMMON is used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Figure 6.

DETAILED DESCRIPTION

Digital Section

Figure 7 shows the Digital Section of the 7135. The 7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

Run/HOLD (Pin 25). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002 clock pulses. It taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as R/\bar{H} is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of auto zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if Run/HOLD is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

STROBE (Pin 26). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going STROBE pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first STROBE pulse goes negative for $\frac{1}{2}$ clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the STROBE goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last STROBE pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional STROBE pulses will be sent until a new measurement is available.

BUSY (Pin 21). BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an overrange). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to

auto-zero when not BUSY, so it may also be considered a $(ZI + AZ)$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received - as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.

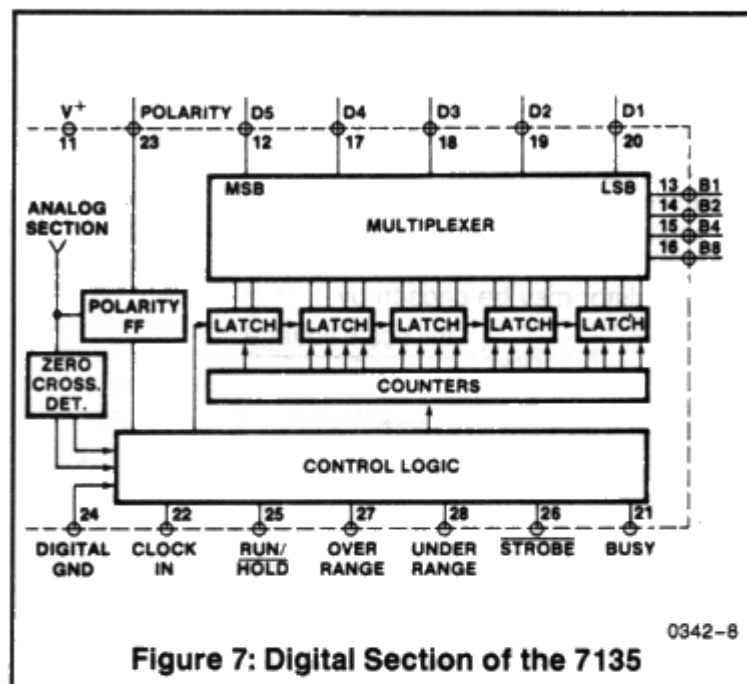


Figure 7: Digital Section of the 7135

OVER-RANGE (Pin 27). This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F/F is set at the end of BUSY and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

UNDER-RANGE (Pin 28). This pin goes positive when the reading is 9% of range or less. The output F/F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.

POLARITY (Pin 23). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (-) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

Digit Drives (Pins 12, 17, 18, 19 and 20). Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D₅ (MSD), D₄, D₃, D₂ and D₁ (LSD). All five digits are scanned and this scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D₅ will start the scan again. This can give a blinking display as a visual indication of over-range.

BCD (Pins 13, 14, 15 and 16). The Binary coded Decimal bits B₈, B₄, B₂ and B₁ are positive logic signals that go on simultaneously with the digit driver signal.

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COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They can supply 20µA of drive current with negligible non-linearity. Values of 5 to 40µA give good results, with a nominal of 20µA, and the exact value of integrating resistor may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

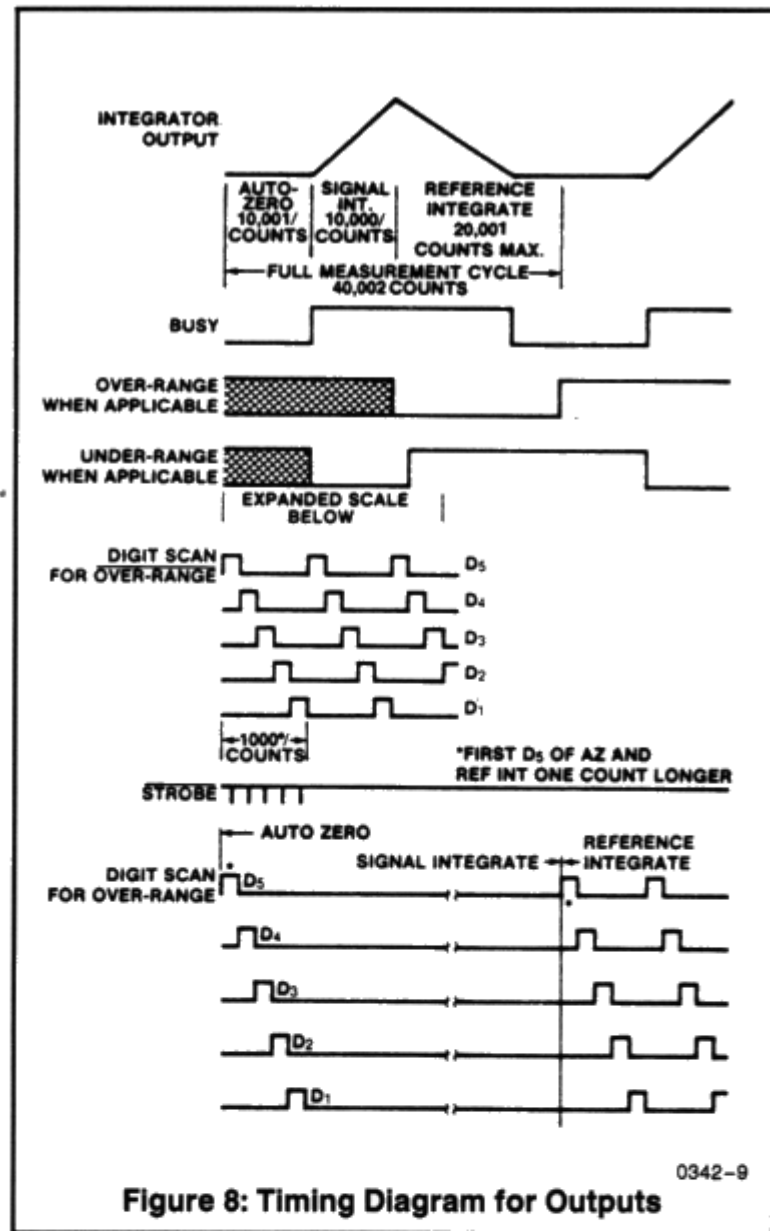
The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance built-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is fine, and 0.47µF is nominal. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{[10,000 \times \text{clock period}] \times I_{INT}}{\text{integrator output voltage swing}}$$

$$= \frac{(10,000) (\text{clock period}) (20\mu A)}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.



Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

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The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2 V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

Rollover Resistor and Diode

A small rollover error occurs in the 7135, but this can be easily corrected by adding a diode and resistor in series between the INTEGRATOR OUTPUT and analog COMMON or ground. The value shown in the schematics is optimum for the recommended conditions, but if integrator swing or clock frequency is modified, adjustment may be needed. The diode can be any silicon diode, such as 1N914. These components can be eliminated if rollover error is not important, and may be altered in value to correct other (small) sources of rollover as needed.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a $3\mu\text{s}$ delay, and at a clock frequency of 160kHz ($6\mu\text{s}$ period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a $50\mu\text{V}$ input, 1 to 2 with $150\mu\text{V}$, 2 to 3 at $250\mu\text{V}$, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to $\sim 1\text{MHz}$ may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant nonlinearities in the first few counts of the instrument - see Application Note A017.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, $33\frac{1}{3}\text{kHz}$, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, $166\frac{2}{3}\text{kHz}$, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

EVALUATING THE ERROR SOURCES

Errors from the "ideal" cycle are caused by:

1. Capacitor droop due to leakage.
2. Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity (dielectric absorption.)
6. Charge lost by C_{REF} in charging C_{stray} .
7. Charge lost by C_{AZ} and C_{INT} to charge C_{stray} .

Each of these errors is analyzed for its error contribution to the converter in application notes listed on the back page, specifically A017 and A032.

NOISE

The peak-to-peak noise around zero is approximately $15\mu\text{V}$ (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately $30\mu\text{V}$. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

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POWER SUPPLIES

The 7135 is designed to work from $\pm 5V$ supplies. However, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ± 1.5 volts.

See "differential input" for a discussion of the effects this will have on the integrator swing without loss of linearity.

TYPICAL APPLICATIONS

The circuits which follow show some of the wide variety of possibilities, and serve to illustrate the exceptional versatility of this A/D converter.

Figure 9 shows the complete circuit for a 4-1/2 digit ($\pm 2,000V$) full scale) A/D with LED readout using the ICL8069 as a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to $50\mu A$. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The 1/2 digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder. The 2-gate clock circuit should use CMOS gates to maintain good power supply rejection.

A suitable circuit for driving a plasma-type display is shown in Figure 10. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'BI' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The $2.5k\Omega$ & $3k\Omega$ resistors set the current levels in the display. A similar arrangement can be used with Nixie® tubes.

The popular LCD displays can be interfaced to the O/P of the ICL7135 with suitable display drivers, such as the ICM7211A as shown in Figure 11. A standard CMOS 4030 QUAD XOR gate is used for displaying the 1/2 digit, the polarity, and an 'overrange' flag. A similar circuit can be used with the ICL7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-1/2 digit ($\pm 2,000V$) A/D.

Figure 12 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the STROBE signal and 'Overrange' is indicated by blanking the 4 full digits.

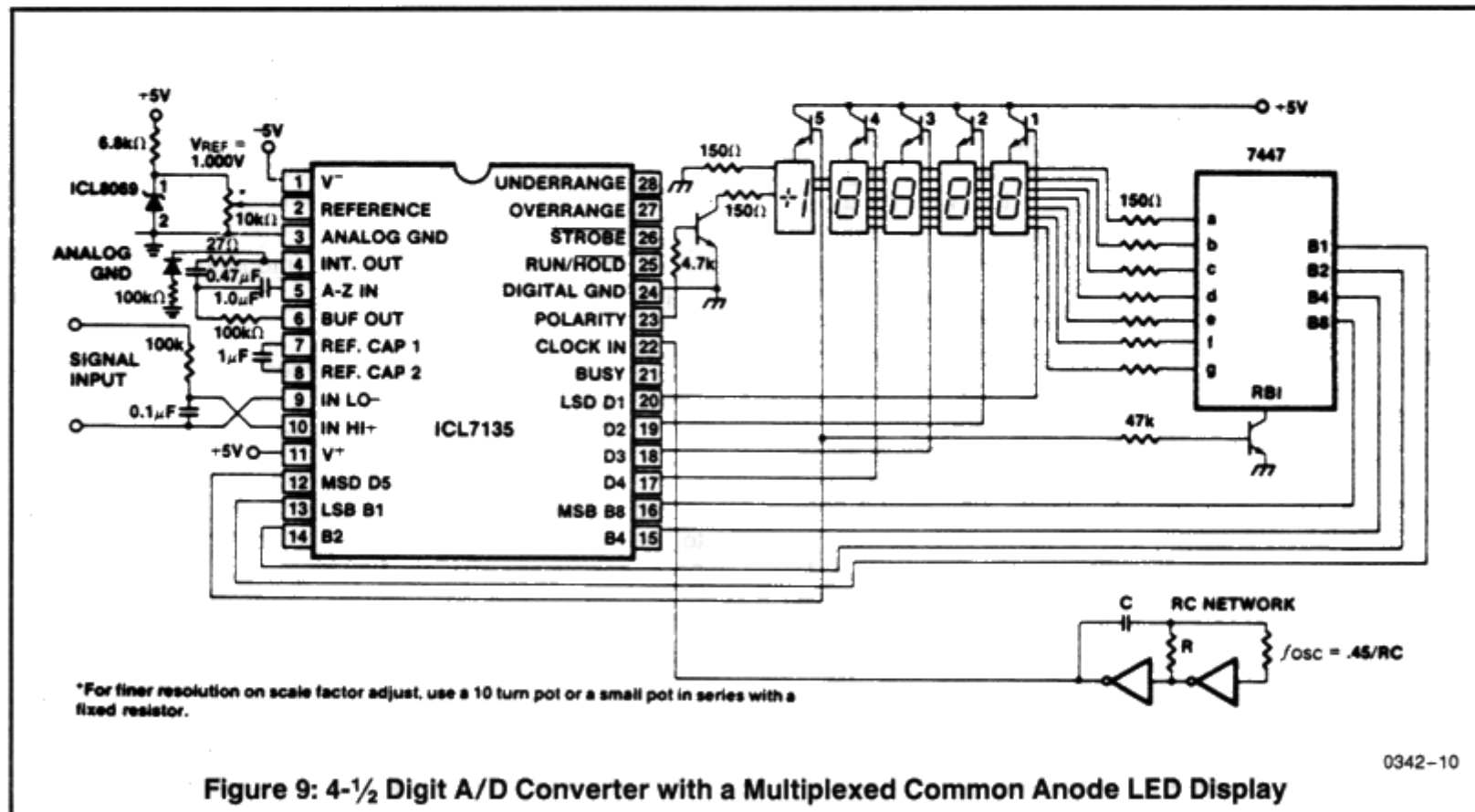


Figure 9: 4-1/2 Digit A/D Converter with a Multiplexed Common Anode LED Display

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NOTE: All typical values have been characterized but are not tested.

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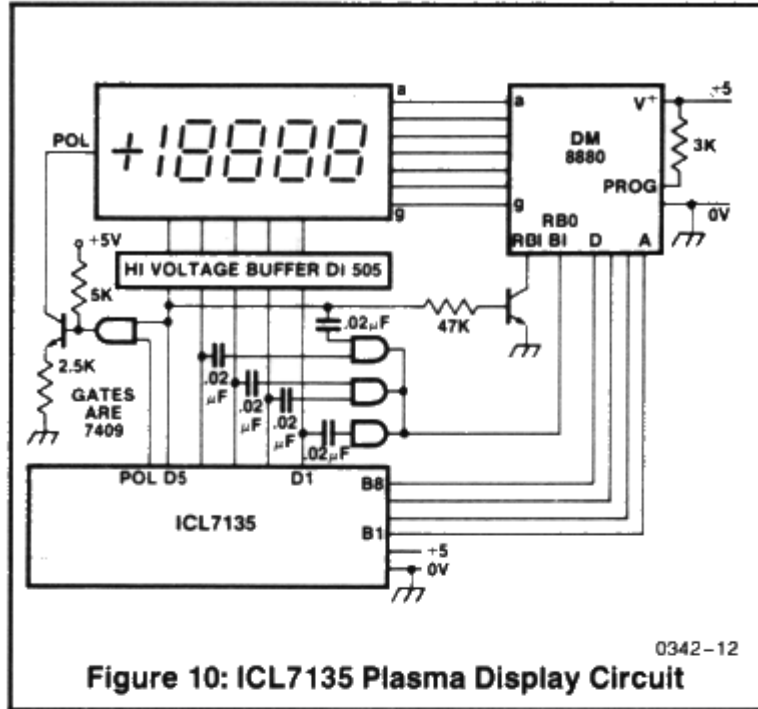


Figure 10: ICL7135 Plasma Display Circuit

0342-12

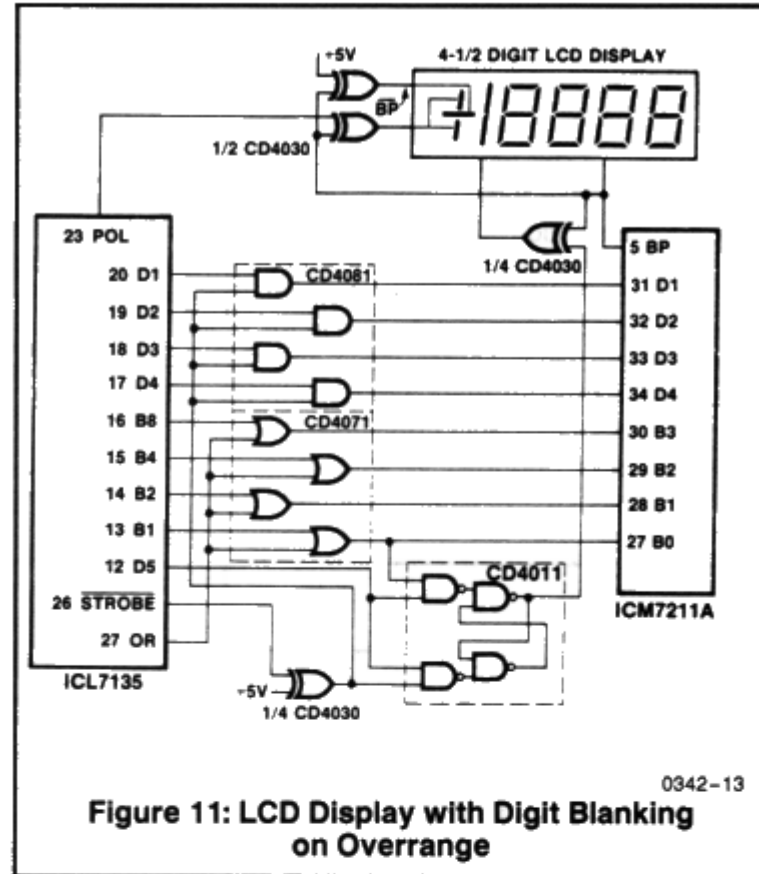


Figure 11: LCD Display with Digit Blanking on Overrange

0342-13

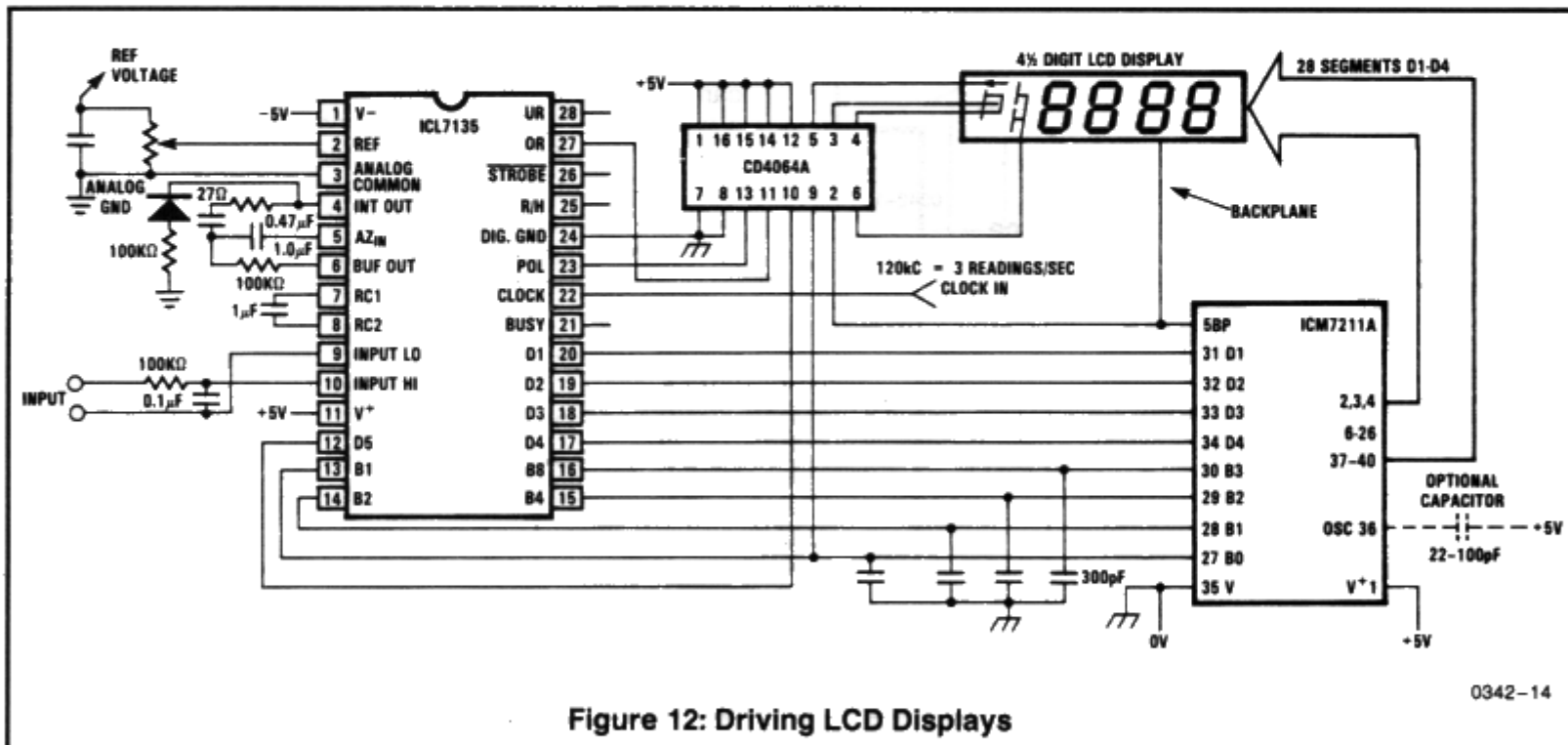


Figure 12: Driving LCD Displays

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A problem sometimes encountered with both LED & plasma-type display driving is that of clock source supply line variations. Since the supply is shared with the display, any variation in voltage due to the display reading may cause clock supply voltage modulation. When in overrange the display alternates between a blank display and the 0000 overrange indication. This shift occurs during the reference integrate phase of conversion causing a low display reading just after overrange recovery. Both of the above circuits have considerable current flowing in the digital supply from drivers, etc. A clock source using an LM311 voltage comparator with positive feedback (Figure 13) could minimize any clock frequency shift problem.

The 7135 is designed to work from ± 5 volt supplies. However, if a negative supply is not available, it can be generated with an ICL7660 and two capacitors (Figure 14).

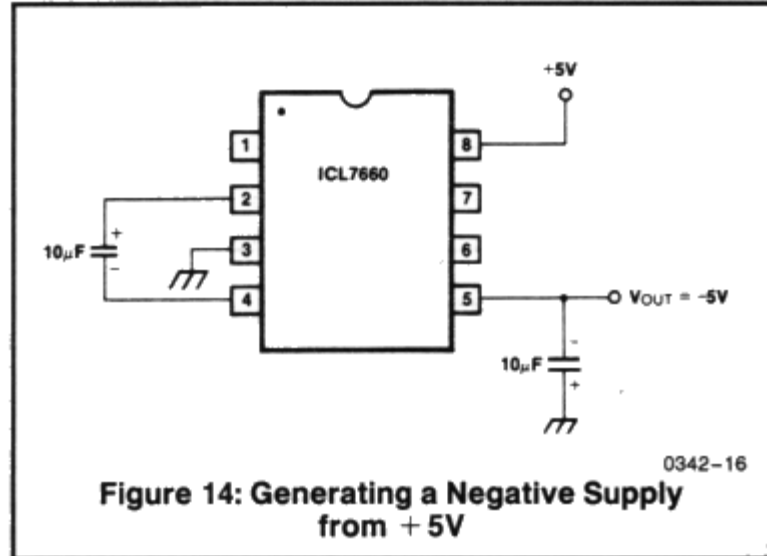


Figure 14: Generating a Negative Supply from +5V

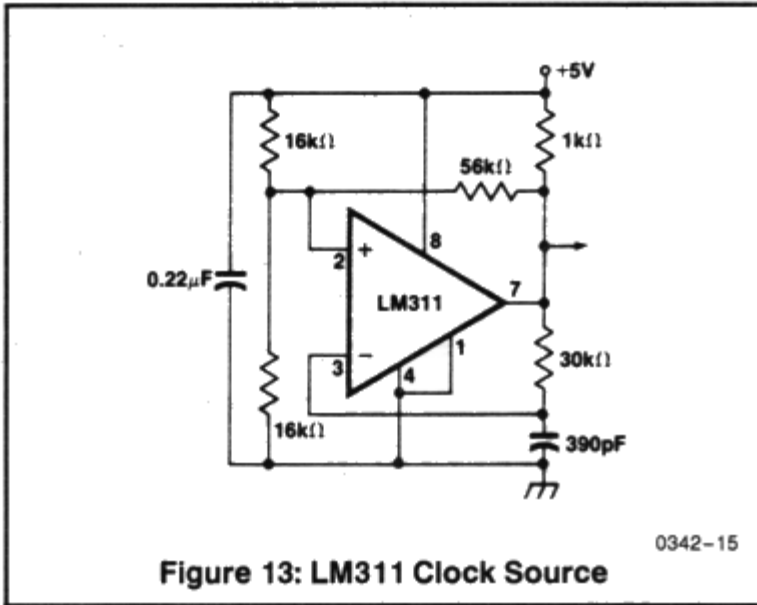


Figure 13: LM311 Clock Source

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 15 shows a very simple interface between a free-running ICL7135 and a UART. The five $\overline{\text{STROBE}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 16. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The BUSY signal resets the Data Ready Reset (DRR). Again $\overline{\text{STROBE}}$ starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

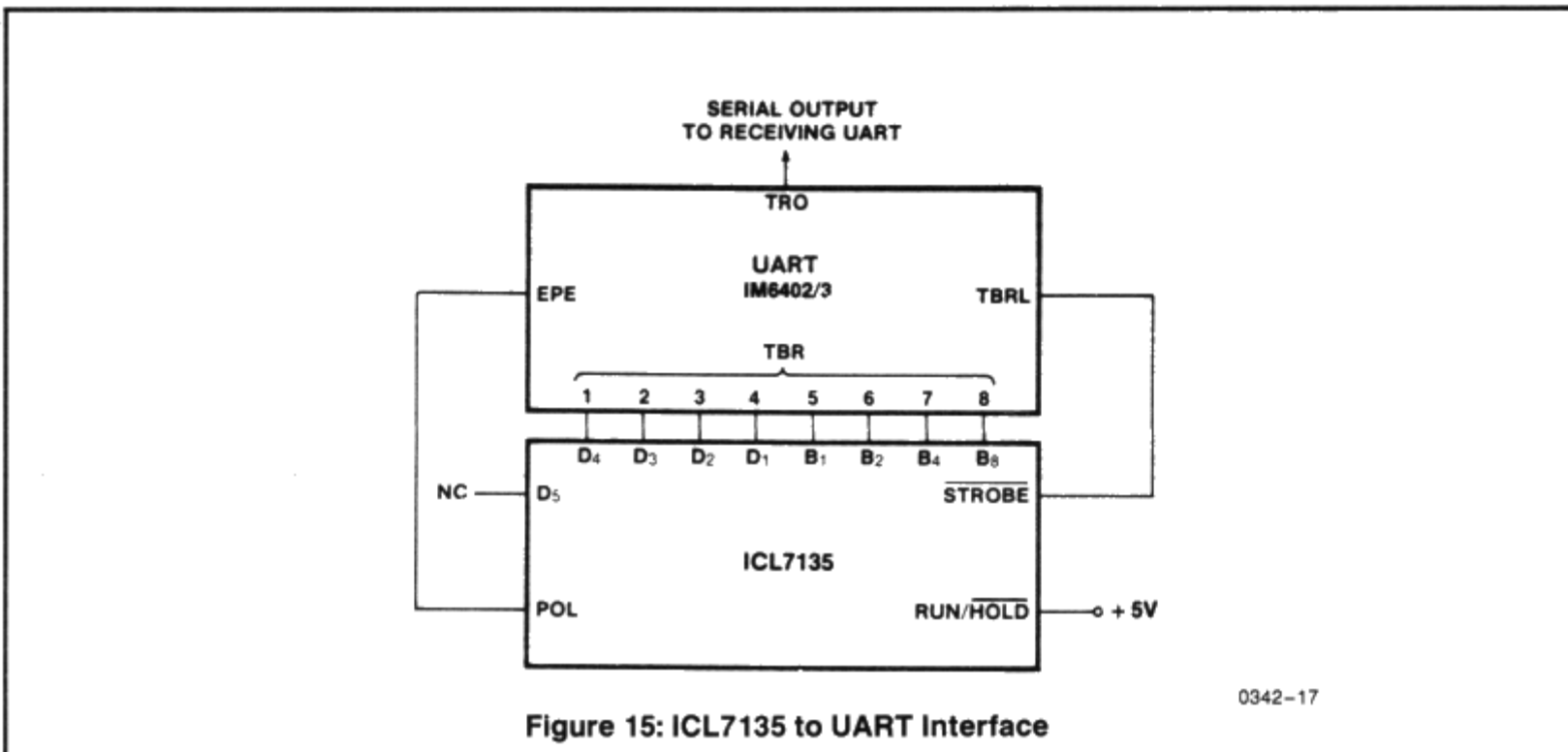


Figure 15: ICL7135 to UART Interface

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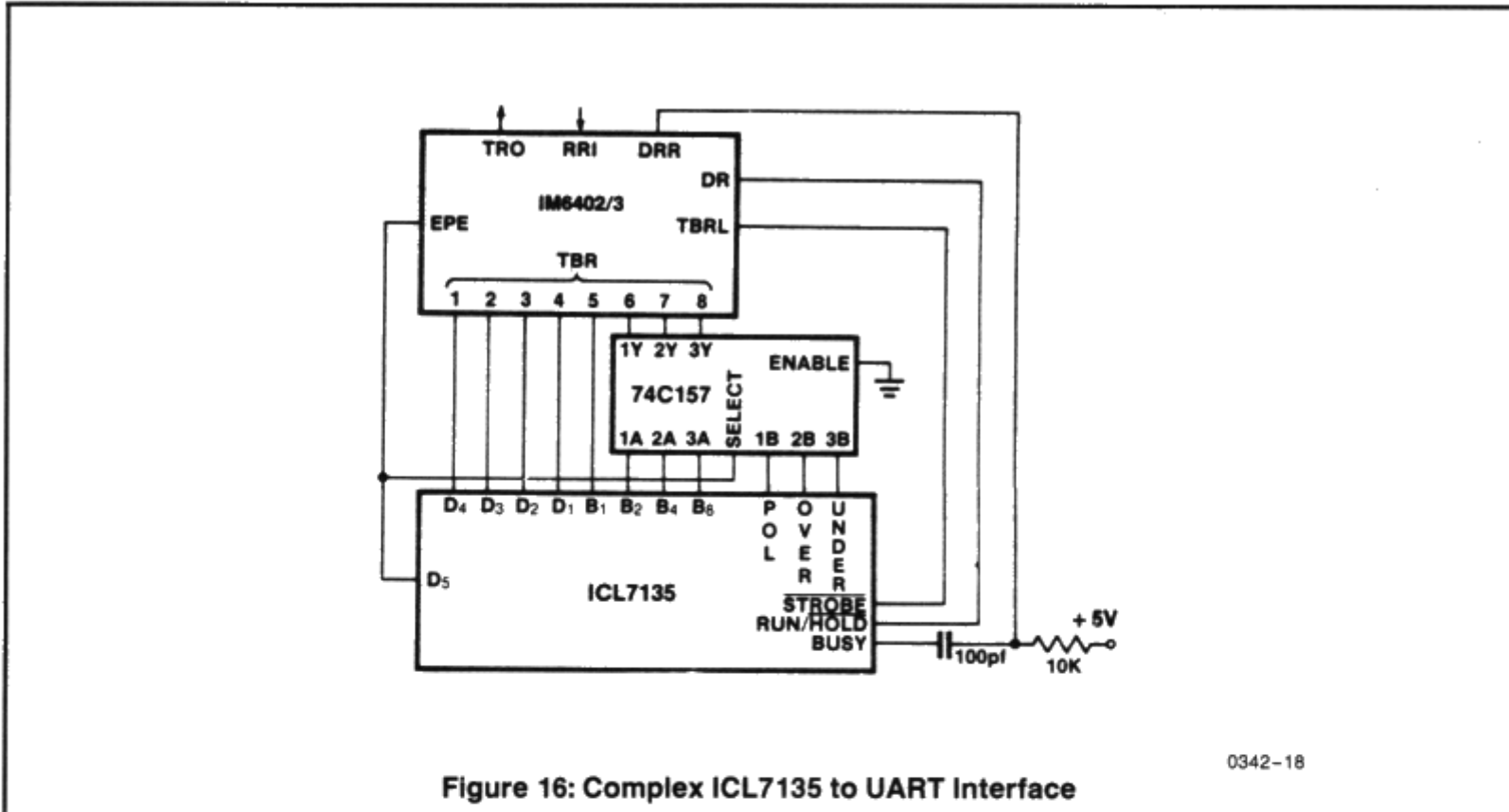


Figure 16: Complex ICL7135 to UART Interface

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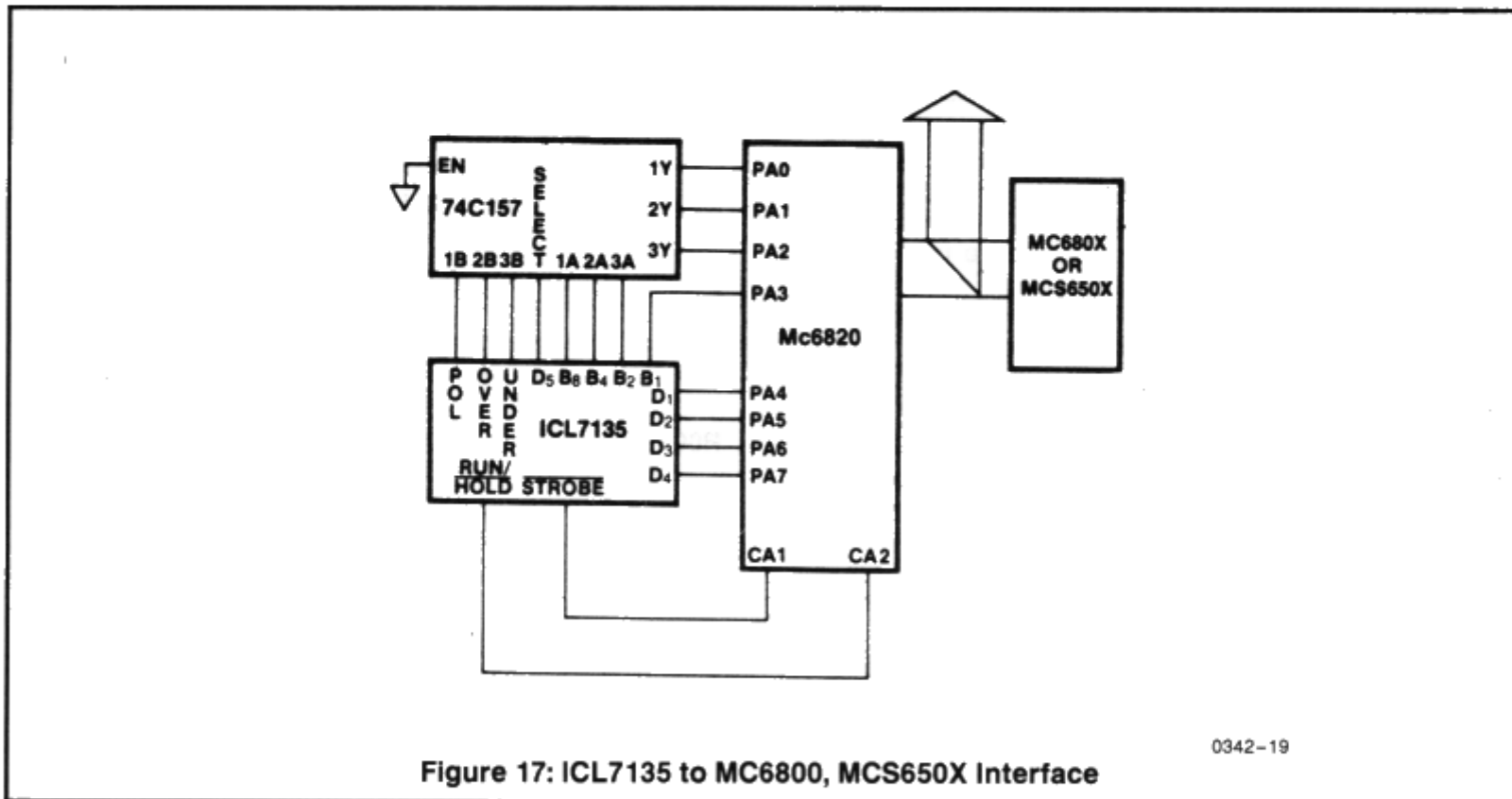


Figure 17: ICL7135 to MC6800, MCS650X Interface

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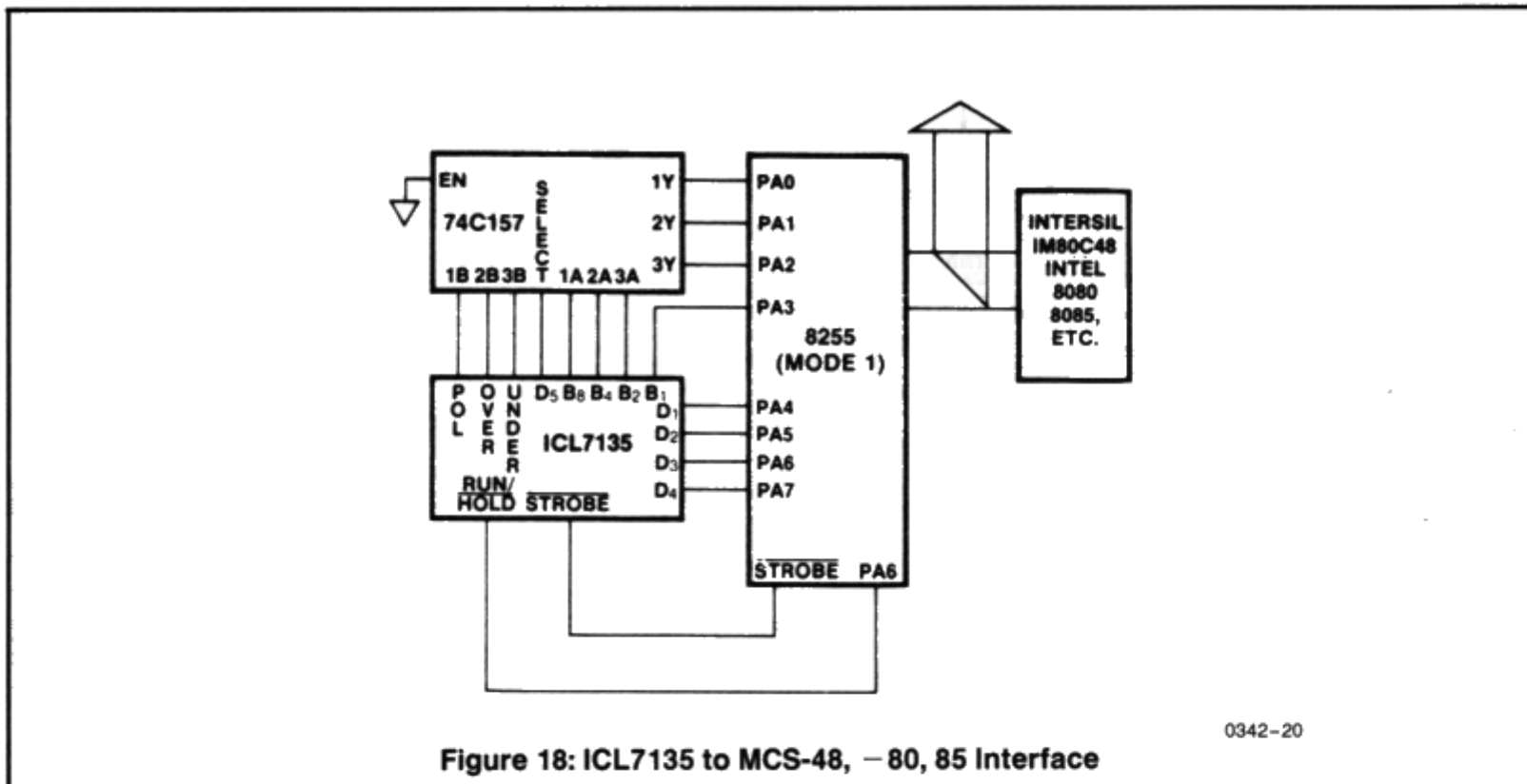


Figure 18: ICL7135 to MCS-48, -80, 85 Interface

0342-20

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next STROBE pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the ICL7135 directly with three popular microprocessors are shown in Figures 17 and 18. The 8080/8048 and the MC6800 groups with 8 bit buses need to have polarity, over-range and under-range multiplexed onto the Digit 5 word — as in the UART circuit. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

APPLICATION NOTES

- A016 "Selecting A/D Converters," by David Fullagar
- A017 "The Integrating A/D Converters," by Lee Evans

- A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
- A019 "4-1/2 Digit Plan Meter Demonstrator/Instrumentation Boards," by Michael Dufort
- A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort
- A028 "Building an Auto-Ranging DMM Using the 8052A/7103A A/D Converter Pair," by Larry Goff
- A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
- A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family", by Peter Bradshaw
- R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

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NOTE: All typical values have been characterized but are not tested.